

| Organization | | | |
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| Legal name: Grenoble INP | Short name: INPG | Department/Faculty/etc.: FMNT/IMEP-LAHC | Partner number: 2 |
| Lecturer | | | |
| Name: BALESTRA | First name: Francis | E-mail address: balestra@minatec.inpg.fr | |
| Title/topic | | | |
| Nanoscale CMOS and Si-based beyond-CMOS nanodevices | | | |
| Short abstract | | | |
| <p><i>The lecture presents new concepts, novel materials and technologies, innovative device architectures needed to overcome the number of challenges for N+4 technology nodes and beyond for CMOS and post-CMOS Nanoelectronics.</i></p> <p><i>The main recent advances on new channel materials (strained layers on bulk and insulator, SiGe, Ge, etc.), novel source-drain architectures, advanced gate stacks and innovative nanodevices (multi-gates, nanowires, nanotubes, etc.) will be presented.</i></p> | | | |

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| Legal name: Grenoble INP | Short name: INPG | Department/Faculty/etc.: FMNT/IMEP-LAHC | Partner number: 2 |
| Lecturer | | | |
| Name: CRISTOLOVEANU | First name: Sorin | E-mail address: sorin@enserg.fr | |
| Title/topic | | | |
| Multiple Gates for SOI MOSFETs: Two, Three or Four ? | | | |
| Short abstract | | | |
| <p><i>The nano-size multiple-gate SOI MOS transistor is the ideal candidate for the microelectronic future, including the transition from micro- to nano-electronics. The MOSFET scaling is intrinsic easier in SOI than in bulk Si, where it is becoming a desperate issue. The key condition is to use ultra-thin bodies and to open the SOI family to any kind of semiconductor, strained or not, on any type of dielectric.</i></p> <p><i>The aim of this presentation is to illustrate the improvement of the electrostatic control achieved by the association of several gates. Two, three or four gates can collaborate for enabling enhanced performance, functionality, flexibility and scaling. Several device architectures (planar or vertical double gates, Ω or Π topologies, 4-gate and gate-all-around transistors) will be discussed comparing their merits and feasibility. Since the device operation is governed by 3-D effects, we will describe the typical coupling mechanisms along the longitudinal, lateral and vertical directions. These devices with multiple addressable gates open a new paradigm in circuit design. Preliminary examples of innovative reconfigurable circuits will be proposed.</i></p> | | | |

| Organization | | | |
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| Legal name: IMEP | Short name: | Department/Faculty/etc.: Grenoble Polytechnic Institute | Partner number: 2 |
| Lecturer | | | |
| Name: CRISTOLOVEANU | First name: Sorin | E-mail address: sorin@enserg.fr | |
| Title/topic | | | |
| Selected Characterization Techniques for SOI Materials and Devices | | | |
| Short abstract | | | |
| <p>SOI is a necessary technology, with multiple facets that need to be correctly captured and understood. The goal of this tutorial is to offer a comprehensive view of the general strategy and dedicated methods for electrical characterization. It is not aimed to provide an exhaustive catalogue of techniques, instead it is designed to be practical and provide helpful guiding for conducting proper measurements.</p> <p>The evaluation of SOI structures is hampered by several problems: thinness of the film, presence of the BOX, stacked interfaces, typical defects, strain, etc. The electrical properties are of uppermost interest as they directly impact on the design and performance of integrated circuits. A number of conventional methods can be borrowed from bulk Si and adapted to SOI whereas other methods are no longer applicable in thin films. Fortunately novel techniques, such as the pseudo-MOS transistor can be conceived and implemented. The ingredients of the pseudo-MOSFET will be described, based on examples demonstrating why it became a successful and efficient routine technique for SOI material evaluation at the wafer level. Several alternatives (Hg-FET, Hall effect, etc) will be addressed.</p> <p>We will next see how to manipulate single-gate and multiple-gate MOSFETs in order to reveal, from their static and dynamic characteristics, key parameters like carrier mobility and lifetime, threshold voltage, self-heating, leakage currents, etc. Various parameter extraction methods for the evaluation of the series resistance, interface traps and oxide defects will be explicated and critically compared. A direct application is the monitoring of radiation-induced damage and hot-carrier reliability effects. More sophisticated techniques like split-CV, geometric magnetoresistance and lowtemperature transport are very successful for universal mobility characterization in very advanced MOSFETs. The charge pumping, transient currents, and noise spectroscopy will also be evoked. We will see the appropriate treatment for multiple channels. Independently, each channel informs on the quality of the nearby interface. The multi-channel coupling effects are more complex and basically have a two-fold impact: they alter the measurement signature but, in turn, they can be taken advantage of for detailed analysis of the physics mechanisms.</p> | | | |

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| Lecturer | | | |
| Name: MOUIS | First name: Mireille | E-mail address: Mireille.Mouis@minatec.inpg.fr | |
| Title/topic | | | |
| Characterization of transport in ultra short field-effect transistors | | | |
| Short abstract | | | |
| <p><i>Carrier mobility is the parameter that is used to characterize transport in long channel field-effect transistors. However, as gate length reaches the 10nm range, its extraction raises conceptual and experimental difficulties. New architectures, such as double-gate MOSFETs or FinFETs raise new characterization challenges too, since several channels may be involved. In this talk, we will discuss the validity of the mobility concept in ultra short transistors. We will show the potential of some transport characterization methods, with new improvements aiming at handling ultra short channels, as well as techniques that study the influence of additional parameters such as strain or magnetic field. The discussion will be illustrated by recent examples obtained on ultra short transistors with advanced architectures (ultra-thin body FD-SOI transistors, double-gate transistors, strained channel devices, etc).</i></p> | | | |

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| Legal name: <i>University of Warwick</i> | Short name: <i>Warwick</i> | Department/Faculty/etc.: <i>Physics</i> | Partner number: <i>03</i> |
| Lecturer | | | |
| Name: <i>Leadley</i> | First name: <i>David</i> | E-mail address: <i>d.r.leadley@warwick.ac.uk</i> | |
| Title/topic | | | |
| <i>Strained layer materials and device properties</i> | | | |
| Short abstract | | | |
| <i>On request</i> | | | |

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| Legal name: <i>University of Warwick</i> | Short name: <i>Warwick</i> | Department/Faculty/etc.: <i>Physics</i> | Partner number: <i>03</i> |
| Lecturer | | | |
| Name: <i>Myronov</i> | First name: <i>Maksym</i> | E-mail address: <i>m.myronov@warwick.ac.uk</i> | |
| Title/topic | | | |
| <i>Epitaxial growth of strained layers</i> | | | |
| Short abstract | | | |
| <i>On request</i> | | | |

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| Legal name: <i>University of Warwick</i> | Short name: <i>Warwick</i> | Department/Faculty/etc.: <i>Physics</i> | Partner number: <i>03</i> |
| Lecturer | | | |
| Name: <i>Parker</i> | First name: <i>Evan</i> | E-mail address: <i>evan.parker@warwick.ac.uk</i> | |
| Title/topic | | | |
| <i>Epitaxial growth of silicon based layers</i> | | | |
| Short abstract | | | |
| <i>On request</i> | | | |

| Organization | | | |
|--|----------------------------------|---|------------------------------------|
| Legal name: <i>Kungl Tekniska Högskolan</i> | Short name: <i>KTH</i> | Department/Faculty/etc.: <i>School of ICT</i> | Partner number: <i>5</i> |
| Lecturer | | | |
| Name: <i>Östling</i> | First name: <i>Mikael</i> | E-mail address: <i>ostling@kth.se</i> | |
| Title/topic | | | |
| <i>High frequency device technology</i> | | | |
| Short abstract | | | |
| <i>This lecture deals with ultimate device scaling with respect to high frequency performance of advanced silicon devices. State of the art processing modules are examined as well as electrical performance of devices. Aspects of low frequency noise are treated. Lecture is planned for one hour.</i> | | | |

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| Lecturer | | | |
| Name: <i>Östling</i> | First name: <i>Mikael</i> | E-mail address: <i>ostling@kth.se</i> | |
| Title/topic | | | |
| <i>Silicides in microelectronics</i> | | | |
| Short abstract | | | |
| <i>This lecture will treat the aspects of utilizing metal silicides in the micro and nanoelectronics device technology. Fundamental aspects of silicide formation including kinetics, formation mechanisms are given. Integration schemes will be discussed and numerous examples of technical solutions are discussed. Lecture is about one hour.</i> | | | |

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| Legal name: <i>Kungliga Tekniska Högskolan</i> | Short name: <i>KTH</i> | Department/Faculty/etc.: <i>School of ICT, Department of Microelectronics and Applied Physics</i> | Partner number: <i>5</i> |
| Lecturer | | | |
| Name: <i>Per-Erik</i> | First name: <i>Hellström</i> | E-mail address: <i>pereh@kth.se</i> | |
| Title/topic | | | |
| <i>Overview of Schottky barrier MOSFETs</i> | | | |
| Short abstract | | | |
| <i>This lecture reviews the latest developments in MOSFETs with Schottky barrier contacts. Key advancements in technology such as choice of metals, dopant segregation and integration will be covered. Potential and status of state-of-the-art Schottky barrier MOSFETs will be described. Lecture is planned for one hour.</i> | | | |

| Organization | | | |
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| Legal name: <i>Università degli Studi di Udine, IUNET</i> | Short name: <i>DIEGM, IUNET</i> | Department/Faculty/etc.: <i>Dipartimento di Ingegneria Elettrica, Gestionale e Meccanica</i> | Partner number: <i>6</i> |
| Lecturer | | | |
| Name: <i>Selmi</i> | First name: <i>Luca</i> | E-mail address: <i>selmi@uniud.it</i> | |
| Title/topic | | | |
| <i>Silicon Nitride – based FLASH Memory devices</i> | | | |
| Short abstract | | | |
| <p><i>FLASH Memory scaling is facing increasing difficulties and new cell concepts may be needed to replace the conventional Floating Gate architecture beyond the 32nm technology node. Among the proposed new concepts, cells which replace the Floating Gate with a localized trapping material (e.g. silicon nitride) are attracting increasing attention. This lecture focuses on silicon nitride based NVM cell concepts (e.g. SONOS, TANOS) with emphasis on the operating principles, the program erase and retention mechanisms, the pros and cons w.r.t. conventional floating gate technology. Characterization, modeling and simulation issues of these promising devices will be discussed based on examples from recent research activities in the field.</i></p> | | | |

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| Legal name: <i>Politecnico di Milano, IUNET</i> | Short name: <i>POLIMI - IUNET</i> | Department/Faculty/etc.: <i>Electronics and Information Technology</i> | Partner number: <i>6</i> |
| Lecturer | | | |
| Name: <i>Spinelli</i> | First name: <i>Alessandro</i> | E-mail address: <i>alessandro.spinelli@polimi.it</i> | |
| Title/topic | | | |
| <i>Reliability issues in advanced non-volatile memories</i> | | | |
| Short abstract | | | |
| <i>Scaled non-volatile memories are facing new reliability issues related to the reduction of their physical dimensions and of the number of electrons used to represent the stored bits. For example, random telegraph noise coupled to random dopant fluctuations, fluctuations in the number of injected electrons, anomalous programming and erasing are new mechanisms which must be accounted for, beyond the traditional concern for SILC and retention issues related to the oxide damage after cycling. The lecture addresses the different concerns for NOR and NAND technologies, and the possibilities offered by innovative concepts for storage.</i> | | | |

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| Lecturer | | | |
| Name: <i>Esseni</i> | First name: <i>David</i> | E-mail address: <i>esseni@uniud.it</i> | |
| Title/topic | | | |
| <i>Transport in advanced CMOS transistors</i> | | | |
| Short abstract | | | |
| <p><i>The high-K gate dielectrics, the crystal orientation and the strain for silicon MOSFETs as well as the use of alternative channel materials have become important design knobs in CMOS technologies, that need being studied and engineered to continue the scaling process. In this framework, the role of physically based modeling is very relevant to steer the technology towards the most promising options. The best crystal orientation and strain configuration, for example, are not the same for the nMOS and pMOS devices, and the understanding of these differences and of their practical implications require again an insight into the way the above design options affect the transport in the channel of the transistors. The lecturer can address different topics concerning the transport modeling in this generalized scaling scenario, at the aim to create a link between the available experimental data, the predictive capabilities of the models and the resulting projections about the device performance and optimization.</i></p> | | | |

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| Legal name: <i>Universita' di Pisa, IUNET</i> | Short name: <i>PISA - IUNET</i> | Department/Faculty/etc.: <i>Dipartimento di Ingegneria dell'Informazione</i> | Partner number: <i>6</i> |
| Lecturer | | | |
| Name: <i>Iannaccone</i> | First name: <i>Giuseppe</i> | E-mail address: <i>g.iannaccone@iet.unipi.it</i> | |
| Title/topic | | | |
| Noise in nanoelectronic transistors | | | |
| Short abstract | | | |
| <p><i>Noise has an increasing role in the operation of nanoscale transistors for two main reasons: First, as device size shrinks, the operation of transistors involves an ever smaller number of electrons, which implies a smaller signal to noise ratio. Second, transistor operation is very sensitive to the presence of single defects. In this talk we will review the specific properties of noise in nanoscale transistors, considering both more moore devices, i.e. aggressively scaled planar and ultrathin body devices, and beyond CMOS devices, such as those base on silicon nanowires and carbon materials.</i></p> | | | |

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| Lecturer | | | |
| Name: <i>Iannaccone</i> | First name: <i>Giuseppe</i> | E-mail address: <i>g.iannaccone@iet.unipi.it</i> | |
| Title/topic | | | |
| <i>Perspectives of multigate transistor architectures for logic and memory</i> | | | |
| Short abstract | | | |
| <i>In this talk we will critically review the perspectives of multiple gate MOSFETs for logic and for non-volatile memories. As far as devices for logic are concerned we will evaluate multigate architectures in terms of i) short channel effects ii) maximum operating frequency iii) intrinsic gain iv) noise properties v) variability vi) packing density. As far as memories are concerned, we will focus on multigate discrete storage memories, such as SONOS and TANOS, focusing on the efficiency of program/erase operation, retention, and packing density.</i> | | | |

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| Lecturer | | | |
| Name: <i>Iannaccone</i> | First name: <i>Giuseppe</i> | E-mail address: <i>g.iannaccone@iet.unipi.it</i> | |
| Title/topic | | | |
| <i>Physical insights into the performance of transistors based on silicon nanowires, carbon nanotubes, or graphene nanostripes</i> | | | |
| Short abstract | | | |
| <p><i>We use three-dimensional simulations of the coupled electrostatics and transport equations to gain insights into the perspective performance of FETs based on silicon nanowires, carbon nanotubes, and graphene nanostripes. Multigate devices ensure very good control of the electrostatics, and therefore open the possibility of channel length scaling in the few nm regime. However, transport properties in quasi-1D channels are extremely sensitive to single defects and rough interfaces. Energy gap variability is also to be expected in particular for the carbon channels, since fabrication or synthesis technology is still very far from precision down to the single atom. We evaluate from the quantitative point of view the impact of defects and variability on the transport properties by using a mix of codes based in the continuum (effective mass approximation) and on an atomistic description (tight-binding hamiltonian).</i></p> | | | |

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| Lecturer | | | |
| Name: <i>Fiori</i> | First name: <i>Gianluca</i> | E-mail address: <i>g.fiori@iet.unipi.it</i> | |
| Title/topic | | | |
| <i>Perspectives and limits of Carbon Electronics</i> | | | |
| Short abstract | | | |
| <p><i>Carbon material is nowadays offering the possibility of exploring one-dimensional systems and relativistic condensed matter physics, and is gaining the limelight in the nanoelectronic field because of its potential to meet ITRS requirements. However, it is still unclear what part such a new material will actually take in the semiconductor industry. The lecturer will address perspectives and limits of carbon devices, focusing the attention on carbon nanotubes, graphene nanoribbon as well as on graphene bilayer field effect transistors.</i></p> <p><i>To this purpose, ideal devices will be investigated in order to outline the best performance to be expected for the different channel materials, while the inclusion of possible source of non-idealities will provide information concerning the sensitivity of carbon based devices to process variations and undesired factors like ionized impurities, defects and line edge roughness in nanoribbons.</i></p> | | | |

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| Legal name: <i>Université Catholique de Louvain</i> | Short name: <i>UCL</i> | Department/Faculty/etc.: <i>Microelectronics Laboratory / Electrical Department</i> | Partner number: <i>7</i> |
| Lecturer | | | |
| Name: <i>Flandre</i> | First name: <i>Denis</i> | E-mail address: <i>denis.flandre@uclouvain.be</i> | |
| Title/topic | | | |
| <i>Novel ultra-low-power CMOS design techniques for analog, digital and memory functions. Implementations in SOI technology</i> | | | |
| Short abstract | | | |
| <i>On request</i> | | | |

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| Lecturer | | | |
| Name: <i>Flandre</i> | First name: <i>Denis</i> | E-mail address: <i>denis.flandre@uclouvain.be</i> | |
| Title/topic | | | |
| <i>SOI CMOS analog : device performance assessment and modelling, circuit design</i> | | | |
| Short abstract | | | |
| <i>On request</i> | | | |

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| Legal name: <i>Université Catholique de Louvain</i> | Short name: <i>UCL</i> | Department/Faculty/etc.: <i>Microwaves Laboratory / Electrical Department</i> | Partner number: <i>7</i> |
| Lecturer | | | |
| Name: <i>Raskin</i> | First name: <i>Jean-Pierre</i> | E-mail address: <i>jean-pierre.raskin@uclouvain.be</i> | |
| Title/topic | | | |
| <i>Wideband characterization of advanced SOI materials and devices: issues and technological solutions</i> | | | |
| Short abstract | | | |
| <i>Based on the extraction of a wideband equivalent small-signal circuit, various MOS technologies will be fairly compared and models with increased validity domain established. Microwave performance of thin-film partially-depleted, fully-depleted SOI MOSFETs as well as multiple gate MOS (MuG) will be assessed. The present limitations of silicon substrates to provide high quality integrated passive elements as well as to reduce the crosstalk and non-linearity generation in mixed-mode IC's will be explained and technological solutions will be exposed. Based on the characterization and modeling of passive and active devices, performance of a few RF circuits such as LNAs, oscillators and RF switches will be presented.</i> | | | |

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| Lecturer | | | |
| Name: <i>Kilchytska</i> | First name: <i>Valeriya</i> | E-mail address: <i>valeriya.kilchytska@uclouvain.be</i> | |
| Title/topic | | | |
| <i>Substrate effects on the dynamic response in SOI MOSFETs, Silicon-on-Nothing devices and FinFETs : measurements, simulations and modelling</i> | | | |
| Short abstract | | | |
| <p><i>Any active or passive device integrated into a SOI technology basically lies on a oxide layer (named BOX for Buried OXide) on top of a silicon substrate. This bilayered structure (BOX-silicon substrate) being underneath each integrated device and circuit, its electrical analysis is of first importance. Moreover, with todays technology downscaling, the coupling through the substrate becomes an important limiting factor for the performance of mixed-mode high-frequency integrated circuits, filters, convertors, transmission lines and even single MOSFETs. This lectrue summarizes the original researches on coupling through the substrate in SOI MOSFETs performed during the last decade at the Université catholique de Louvain (UCL). The influence of technology downscaling on the parasitic substrate coupling is particularly emphasized. Silicon-on-Nothing (SON) and FinFET device architectures are described as efficient engineering solutions, which allow suppressing the substrate-related degradation in the device behaviour. A new alternative technological approach for “true” SON fabrication based on the Si layer transfer over the pre-defined cavities developed at UCL is presented.</i></p> | | | |

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| Lecturer | | | |
| Name: <i>Kilchytska</i> | First name: <i>Valeriya</i> | E-mail address: <i>valeriya.kilchytska@uclouvain.be</i> | |
| Title/topic | | | |
| <i>Specific features of advanced SOI technologies for high-temperature applications</i> | | | |
| Short abstract | | | |
| <p><i>One of the main markets for silicon-on-insulator (SOI) devices is high-temperature application. In the last decade, the technology advances to deep submicron era to improve device performance, lower power consumption, reduce occupied area, etc. This unavoidably results in the appearance of new phenomena or significant changes to existing ones. The question to be addressed is “how the progress in MOSFET technology affects the high-temperature behavior of the devices?” Indeed, progress in technology does not mean simply device shortening, which is directly related to gate oxide thinning, doping level change, introduction of highK/metal gate stacks, but in the same time requests an introduction of new solutions for the control of short-channel effects, as e.g. channel engineering (additional HALO or pocket implantation) and various multiple-gates device architectures. This lecture summarizes our experimental and simulation results obtained on different advanced technologies. We start from FD and PD advanced SOI technologies and finish with multiple-gate MOSFETs. The main attention is focused on temperature dependence of two major MOSFET parameters as threshold voltage and subthreshold slope and its evolution with technology advance. Some exotic effects in advanced devices and their temperature dependences is also briefly shown. It is demonstrated that advanced devices appear to have a great potential for future high temperature application and are worth of further detailed investigations of their high-temperature stability and reliability.</i></p> | | | |

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| Legal name: CEA | Short name: CEA | Department/Faculty/etc.: DSM-INAC-SPSMS- LaTEQS | Partner number: 9 |
| Lecturer | | | |
| Name: Sanquer | First name: Marc | E-mail address: marc.sanquer@cea.fr | |
| Title/topic | | | |
| New concepts and new devices for microelectronics: Quantum transport and Coulomb blockade in silicon nanodevices | | | |
| Short abstract | | | |
| <p><i>This 5 hours lecture covers the field of interference and charge effects appearing in quantum mesoscopic physics, with a particular emphasis on silicon nanodevices. It is illustrated with experimental results by the author in devices obtained through collaboration with LETI and ST. Interference effect and electronic localization, Landauer formulae, Resonant tunneling, ballistic and diffusive transport, Coulomb Blockade (orthodox theory and quantum confinement effects) are discussed. This lecture is given jointly with Dr. Jacques Gautier (CEALETI) which covers applications of quantum mechanics and Single electron charging effect in silicon devices (4 hours). The audience is typically PhD students in micro and nanoelectronics.</i></p> | | | |

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| Legal name: IEMN-ISEN | Short name: IEMN-ISEN | Department/Faculty/etc.: Silicon Microelectronics Group | Partner number: 11 |
| Lecturer | | | |
| Name: Dubois | First name: Emmanuel | E-mail address: emmanuel.dubois@isen.iemn.univ-lille1.fr | |
| Title/topic | | | |
| Low Schottky barrier source-drain contacts | | | |
| Short abstract | | | |
| <p><i>Among the main difficulties to overcome toward the 10 nm gate length MOSFET, many challenges are associated to the source/drain (S/D) extensions. The tight constraints of dopant activation to achieve very highly doped junctions, extremely steep lateral profiling, low contact specific resistance have motivated a renewed interest in MOSFETs architectures that integrate metallic Schottky S/D. Based on that background, metallic Schottky-Barrier-like MOSFETs offer the potential to solve critical problems associated to the source/drain architecture and more specifically due to the specific contact resistance at the metal (or silicide) to silicon interface. In this lecture, specific requirements associated to the S/D module of deeply scaled MOSFETs will be first emphasized. As improved performance of SB-MOSFETs are expected from a tight control of the Schottky interface to produce sub 0.1 eV barriers, a special focus will be put on material considerations, including basic modeling of the Schottky junction, transport modelling and associated extraction methodology of low Schottky barriers. Barrier modulation methods will be reviewed to point out the most appropriate technique based on low temperature dopant segregation. Constraints associated to silicide integration in a practical MOSFET S/D module will be outlined. Finally, results of device integration will be discussed and electrical performance will be benchmarked against state-of-the-art bulk and SOI technologies.</i></p> | | | |

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| Legal name: IEMN-ISEN | Short name: IEMN-ISEN | Department/Faculty/etc.: Silicon Microelectronics Group | Partner number: 11 |
| Lecturer | | | |
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| Title/topic | | | |
| Process simulation for advanced stress and junction engineering | | | |
| Short abstract | | | |
| <p><i>For CMOS devices downscaling, sharp requirements have been defined by the International Technology Roadmap for Semiconductors (ITRS) in terms of drive and off state current and power density, making the geometric scaling a challenging task. The new vector largely adopted to extend Moore's law is the mobility enhancement through the introduction of stress by several techniques (Stress Liner, eSiGe embedded stressor, stress memorization). On the other side, a challenging experimental trade-off is being made on junction processing to meet the sharp requirements in terms of resistance, abruptness and depth. Standard techniques (implantation and rapid thermal annealing) are being pushed to their limits whereas alternative techniques such as preamorphization, solid phase epitaxy (SPE), laser annealing and plasma doping are being optimized. As will be shown in this tutorial, many challenges are being faced by characterisation methods and metrology to support all of this intense research competition. TCAD more generally, and process simulation in particular, have a complementary role to play to identify trade-off and evaluate the scalability.</i></p> | | | |

| Organization | | | |
|--|----------------------------------|---|-------------------------------------|
| Forschungszentrum <i>Juelich</i> | Short name: <i>FZJ</i> | Department/Faculty/etc.: <i>IBN1-IT</i> | Partner number: <i>14</i> |
| Lecturer | | | |
| <i>Mantl</i> | <i>Siegfried</i> | <i>s.mantl@fz-juelich.de</i> | |
| Title/topic | | | |
| <i>High mobility channel materials</i> | | | |
| Short abstract | | | |
| <i>Fabrication of sSOI, structural and electrical properties, stressor methods sSOI devices.</i> | | | |

| Organization | | | |
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| Legal name: <i>Technical University Braunschweig</i> | Short name: <i>TUBS</i> | Department/Faculty/etc.: <i>Institute for Electron Devices and Circuits</i> | Partner number: <i>16</i> |
| Lecturer | | | |
| Name: <i>Meinerzhagen</i> | First name: <i>Bernd</i> | E-mail address: <i>b.meinerzhagen@tu-bs.de</i> | |
| Title/topic | | | |
| <i>Modeling of noise and quantum corrections for device simulations</i> | | | |
| Short abstract | | | |
| <i>On request</i> | | | |

| Organization | | | |
|---|------------------------------|---|-------------------------------------|
| Legal name: UNIVERSITAET STUTTGART | Short name: USTUTT | Department/Faculty/etc.: Institut für Halbleitertechnik | Partner number: 17 |
| Lecturer | | | |
| Name: Kasper | First name: Erich | E-mail address: kasper@iht.uni-stuttgart.de | |
| Title/topic | | | |
| <ul style="list-style-type: none"> - Silicon monolithic mm-wave integrated circuits - SiGe virtual substrates: Growth and applications - Silicon based optoelectronics | | | |
| Short abstract | | | |
| <p><i>Material scaling now accompanies the dimension scaling which drives Moore's law. An essential component of material scaling into the nanometer regime is given by silicon based heterostructures. Molecular beam epitaxy is a versatile research tool to realize different types of heterostructures with vertical dimensions down to 1 nm.</i></p> <p><i>The different topics concern handling of lattice mismatched heterostructures and their application in high frequency and optoelectronics/ microelectronics integration.</i></p> | | | |

| Organization | | | |
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| Legal name: National Center for Scientific Research "Demokritos" | Short name: NCSR "Demokritos" | Department/Faculty/etc.: Institute of Microelectronics (IMEL) | Partner number: 18 |
| Lecturer | | | |
| Name: Nassiopoulou | First name: Androula | E-mail address: A.Nassiopoulou@imel.demokritos.gr | |
| Title/topic | | | |
| Ordering of Si nanocrystals in 2-D layers for nanodot memory devices | | | |
| Short abstract | | | |
| <p><i>Semiconductor nanocrystals memories (NCMs) are composed of a two-dimensional nanocrystal layer embedded within the gate dielectric of a MOSFET structure. Their static and dynamic properties are strongly related with the size and density of the nanocrystals in the nanocrystal layer.</i></p> <p><i>Lateral ordering of the arrays of dots in the two-dimensional dots layer shows important advantages compared with the case of non-ordered structures, which are related with the influence of dots size and density on the electrical characteristics of the memory.</i></p> <p><i>A technology has been developed at IMEL for growing laterally ordered Si nanocrystals embedded in SiO₂ thin layers by using very low energy ion implantation through anodically grown alumina films on oxidized Si substrate.</i></p> | | | |

| Organization | | | |
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| Legal name: Tyndall National Institute, University College Cork | Short name: Tyndall | Department/Faculty/etc.: MicroNano Electronics | Partner number: 19 |
| Lecturer | | | |
| Name: Colinge | First name: Jean- Pierre | E-mail address: jean- pierre.colinge@tyndall.ie | |
| Title/topic | | | |
| SOI Technology | | | |
| Short abstract | | | |
| SOI Materials, the SOI MOSFET, Multigate SOI MOSFETs, Radiation and temperature effects, SOI circuits. | | | |

| Organization | | | |
|--|-----------------------------|--|---------------------------|
| Legal name: Universitat Rovira I Virgili | Short name: URV | Department/Faculty/etc.: Department of Electronic, Electrical and Automatic Control Engineering | Partner number: 21 |
| Lecturer | | | |
| Name: Iñiguez | First name: Benjamin | E-mail address: Benjamin.iniguez@urv.cat | |
| Title/topic | | | |
| Compact modeling of SOI and Multiple Gate MOS devices | | | |
| Short abstract | | | |
| <p><i>This lecture presents and explains compact modeling techniques which have been applied for different types of SOI and multiple-gate MOSFETs (Double-Gate MOSFETs, Gate All Around MOSFETs, FinFETs). Long channel models are obtained by deriving a unified charge control model from the solution the 1-D Poisson's equation in the direction perpendicular to the channel, and using an appropriate transport model. Several techniques have been proposed to incorporate short-channel effects to this unified model. These techniques are based in considering the electrostatic potential as the sum of two contributions: the solution of the 1-D Poisson's equation and a solution of the remaining 2-D or 3-D equation, which is solved, with several approximations, using different methods. Finally, using the active transmission line approach, the compact models are extended to the high frequency operation, in order to study the RF performance, including noise.</i></p> | | | |

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| Legal name: <i>University of Granada</i> | Short name: <i>UGR</i> | Department/Faculty/etc.: <i>Electronics and Computer Science</i> | Partner number: <i>21</i> |
| Lecturer | | | |
| Name: <i>Gamiz</i> | First name: <i>Francisco</i> | E-mail address: <i>fgamiz@ugr.es</i> | |
| Title/topic | | | |
| <i>Mobility in multigate MOSFETs</i> | | | |
| Short abstract | | | |
| <p><i>We analyze the behavior of electron and hole mobility in different multigate structures comprising double gate transistors, FinFETs, and silicon nanowires, with different crystallographic orientations and channel materials. The effect of technological parameters on carrier mobility is broadly analyzed, and its behaviour physically explained. Our main goal is to show how mobility in multiple gate devices compares to that in single gate devices and to study different approaches to improving the mobility in these devices, such as different crystallographic orientations, strained Si channels, Ge channels, etc. We considered two kinds of multiple gate devices: quantum-well based devices, and quantum-wire based devices. The first part is devoted to the first group of devices, where carriers are confined in only one dimension but can move freely in the other two dimensions. The second part focuses on multigate silicon nanowires, where carrier confinement is produced in two dimensions. In this case, carriers are drifted in the other dimension. The different nature of these two types of device led us to develop different approaches to study the electrostatics and transport in each device.</i></p> | | | |

| Organization | | | |
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| Legal name: <i>Chalmers tekniska högskola</i> | Short name: <i>Chalmers</i> | Department/Faculty/etc.: <i>Microtechnology and Nanoscience</i> | Partner number: <i>22</i> |
| Lecturer | | | |
| Name: <i>Olof Engstrom</i> | First name: <i>Olof</i> | E-mail address: <i>olof.engstrom@mc2.chalmers.se</i> | |
| Title/topic | | | |
| <i>Searching for the High-k-Grail</i> | | | |
| Short abstract | | | |
| <i>Navigation in the periodic system to find the final high-k-solution</i> | | | |

| Organization | | | |
|--|---------------------------------------|---|-------------------------------------|
| Legal name: <i>Chalmers tekniska högskola</i> | Short name: <i>Chalmers</i> | Department/Faculty/etc.: <i>Microtechnology and Nanoscience</i> | Partner number: <i>22</i> |
| Lecturer | | | |
| Name: <i>Olof Engstrom</i> | First name: <i>Olof</i> | E-mail address: <i>olof.engstrom@mc2.chalmers.se</i> | |
| Title/topic | | | |
| <i>High-k/silicon interfaces</i> | | | |
| Short abstract | | | |
| <i>The nature of charge carrier energy states and traps at the interface between high-k-dielectrics and silicon.</i> | | | |

| Organization | | | |
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| Legal name: <i>Ecole Polytechnique Fédérale de Lausanne</i> | Short name: <i>EPFL</i> | Department/Faculty/etc.: <i>STI/IEL/Nanolab</i> | Partner number: <i>23</i> |
| Lecturer | | | |
| Name: <i>Ionescu</i> | First name: <i>Adrian</i> | E-mail address: <i>adrian.ionescu@epfl.ch</i> | |
| Title/topic | | | |
| <i>Abrupt electronic switches: from device principles to circuit design</i> | | | |
| Short abstract | | | |
| <p>This lecture particularly addresses the challenges and opportunities offered by nanoelectronic switches with subthreshold swing better than 60mV/decade, in terms of power savings and new functionality. It focuses on new device principles and their illustration, as it follows: (i) solid-state abrupt switches such as tunnel-FET, impact ionization MOS transistor (IMOS) and punchthrough impact ionization MOS transistor (PIMOS) and (ii) non-pure electronic devices combining micro/nano-mechanical movable parts and semiconductor device principles, such as Suspended Gate – FET or Movable Body FET and (iii) ferroelectric FETs. The basic principles are discussed and the state of the art in the field is reviewed. Particular attention is provided to the analysis of true benefits at circuit and system levels resulting from the use of small swing devices and the need for accompanying the technology and device effort by adapted design and/or new system architectures. Some examples concerning power management schemes based on abrupt switches are detailed.</p> | | | |

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| Legal name: <i>Swiss Federal Institute of Technology</i> | Short name: <i>ETHZ</i> | Department/Faculty/etc.: <i>Integrated Systems Laboratory</i> | Partner number: <i>24</i> |
| Lecturer | | | |
| Name: <i>Schenk</i> | First name: <i>Andreas</i> | E-mail address: <i>schenk@iis.ee.ethz.ch</i> | |
| Title/topic | | | |
| <i>Quantum Simulation of Silicon Nanowires</i> | | | |
| Short abstract | | | |
| <p><i>Silicon nanowires are perspective core components of future integrated circuits. The feasibility of Si nanowire FETs has been demonstrated by several groups. TCAD-oriented simulation tools can accompany the sophisticated fabrication process, providing aid for performance improvement, supporting the basic understanding, and facilitating the development of new structures. Nanowire FETs with small cross sections and ultra-short gates call for a three-dimensional quantum mechanical treatment of carrier transport beyond the effective mass approximation (EMA). As long as inelastic scattering is neglected, a Wave Function approach is the method of choice due to its numerical advantage over the Non-Equilibrium Green's Function technique. However, the computational burden does not allow to treat important effects like phonon scattering and gate tunneling on a full-band (FB) level. These phenomena still require the EMA. We describe a FB quantum transport simulator and show FB and EMA simulation results for quantum-ballistic currents in Si nanowire FETs focusing on the effects of channel orientation, surface roughness, strain, and direct gate tunneling leakage.</i></p> | | | |

| Organization | | | |
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| Legal name: SYNOPSIS Switzerland LLC | Short name: SNPS | Department/Faculty/etc.: CH10 | Partner number: 25 |
| Lecturer | | | |
| Name: Bufler | First name: Fabian | E-mail address: bufler@synopsys.com | |
| Title/topic | | | |
| Monte Carlo Stress Engineering of Scaled (110) and (100) Bulk pMOSFETs | | | |
| Short abstract | | | |
| <p><i>Bulk pMOSFET performance enhancement by combinations of SiGe pockets, compressively stressed cap liner and (110) surface orientation is investigated by mechanical stress and Monte Carlo device simulation. In agreement with recent measurements, the on-current gain by a (110) surface orientation of the 45 nm pMOSFET with a 3 GPa compressive cap liner is 32 % and 16 % without and with the presence of Si_{0.8}Ge_{0.2} pockets, respectively. However, the performance enhancement by a (110) surface orientation strongly decreases upon scaling and for increasing liner stress. This suggests that the enhanced mobility for (110) surface orientation may lose its advantage in the limit of further scaling and increasing stress.</i></p> | | | |

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| Legal name: <i>The University of Glasgow</i> | Short name: <i>GU</i> | Department/Faculty/etc.: <i>Device Modeling Group</i> | Partner number: <i>26</i> |
| Lecturer | | | |
| Name: <i>Asenov</i> | First name: <i>Asen</i> | E-mail address: <i>A.Asenov@elec.gla.ac.uk</i> | |
| Title/topic | | | |
| <i>Simulation of statistical variability in nano CMOS devices</i> | | | |
| Short abstract | | | |
| <i>Intrinsic parameter fluctuations associated with discreteness of charge and atomicity of matter are now one of the major factors limiting scaling, integration and the reduction of supply voltages and power consumption. The lectures will present recent advances in the simulations atomic scale variability fluctuations in nano CMOS devices using Drift Diffusion (DD), Monte Carlo (MC) and Quantum Transport (QT) techniques.</i> | | | |

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| Legal name: <i>University of Liverpool</i> | Short name: <i>LIVUNI</i> | Department <i>Electrical Engineering & Electronics</i> | Partner number: <i>27</i> |
| Lecturer | | | |
| Name: <i>Hall</i> | First name: <i>Steve</i> | E-mail address: <i>s.hall@liv.ac.uk</i> | |
| Title/topic | | | |
| <i>Oxidation for sub 100nm technology</i> | | | |
| Short abstract | | | |
| <p><i>The aim of this module is to provide delegates with a description of the electronic properties of dielectrics and their on the properties of MOS and other semiconductor devices. It includes discussions of growth methods and kinetics, scaling, reliability and techniques for the study of insulating films as they influence the performance of MOS bulk and SOI devices</i></p> <p><i>On successful completion of this module delegates will have gained an appreciation of the fundamental mechanisms controlling the formation of oxides; an understanding of the measurement of thickness and such electrical properties as density of interface states; a knowledge of conduction properties and trapping effects within the film; a knowledge of ion migration and the relationship to degradation; an in depth appreciation of the relationship of dielectric physical and electrical properties to real integrated devices; an overview of future trends of gate oxides for decananometer CMOS processes including high-K replacements for silicon dioxide.</i></p> | | | |

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| Legal name: <i>University of Newcastle upon Tyne</i> | Short name: <i>UNEW</i> | Department/Faculty/etc.: <i>Electrical, Electronic and Computer Engineering</i> | Partner number: <i>28</i> |
| Lecturer | | | |
| Name: <i>Cowern</i> | First name: <i>Nick</i> | E-mail address: <i>nick.cowern@ncl.ac.uk</i> | |
| Title/topic | | | |
| <i>Doping kinetics in Si and Ge</i> | | | |
| Short abstract | | | |
| <i>On request</i> | | | |