WP3
Joint Processing Platform

Final Review May 26, 2011

Coordinator: Mikael Östling

Presentation: Per-Erik Hellström

JPP Objectives

1. Device processing for FPs in WP1 and WP2
2. Ensure 3,5 month turn-around-time
3. Coordinate processing involving several partners
4. Fabricate MOSFETs and structures for WP4
5. Integrate process modules developed in FPs into JPP's MOSFETs process

WP3 TASKS

3.1 Batch processing for Flagship Projects in WP1 and WP2

3.2 Internal Process Homepage

3.3 Development of process modules for integration in MOSFET process

3.4 Fabrication of MOSFETs and test structures for WP4

Today's presentation

1. Milestones and Deliverables
2. Integrated Process Modules
3. MOSFET batches
4. Summary

WP3 Deliverables

D3.1 Evaluation report on the internal webpage in task 3.2 **(M12)**

D3.2 Report in integrated proocess modules in task 3.3 **(M18)**

D3.3 Report on devices processed in task 3.1 and 3.4 **(M18)**

D3.4 Report in integrated proocess modules in task 3.3 **(M38)**

D3.5 Report on devices processed in task 3.1 and 3.4 **(M38)**

WP3 Milestones

M3.1 Process webpage online **(M6)**

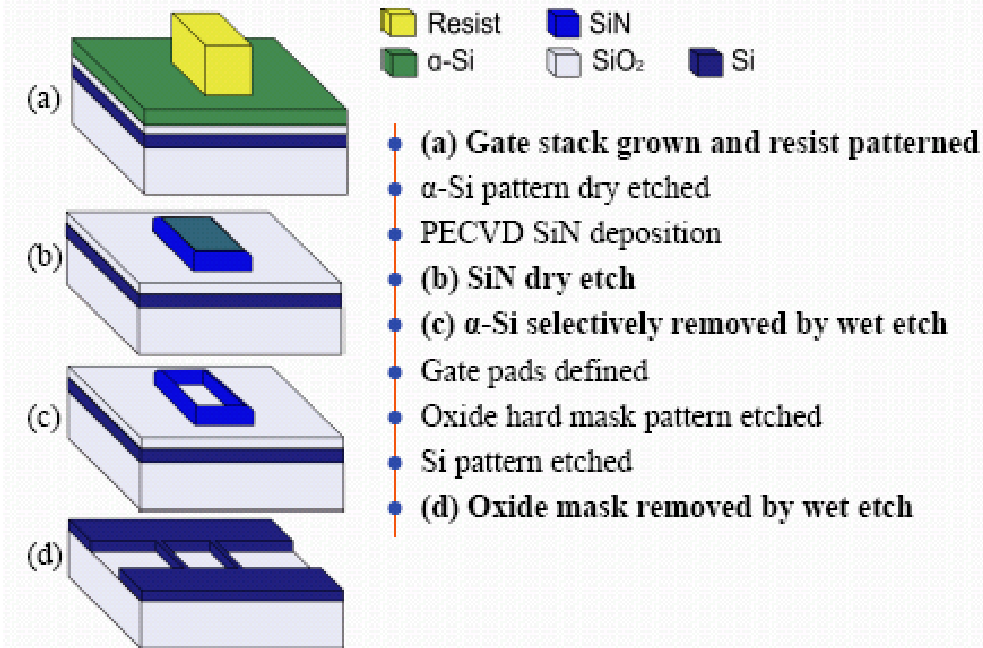
M3.2 Fabrication of new channel materials on SOI for device processing. **(M18)**

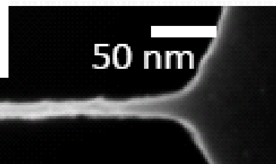
M3.3 Development of a low temperature process **(M18)**

Process Modules

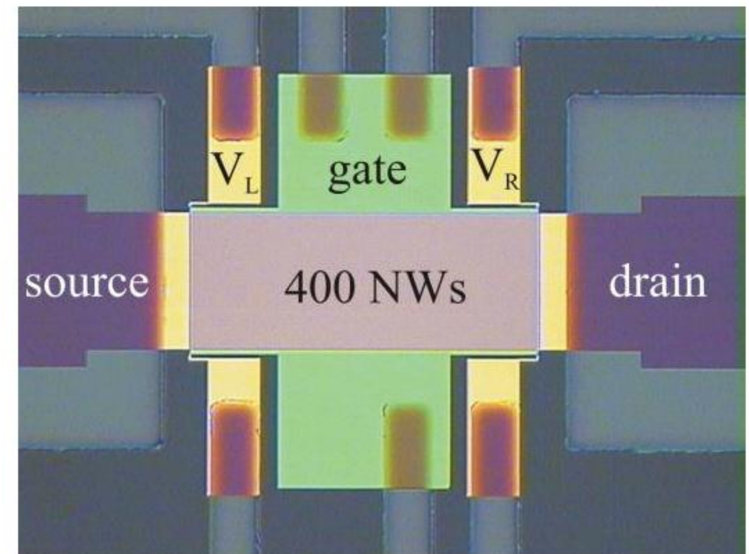
1. Strained SOI wafers
2. Strained Ge wafers
3. Dopant segregated Schottky Barrier S/D technology
4. $LaLuO_3$/TiN gate stack
5. Silicon nanowire process

Top-down Si nanowires





e-beam lithography



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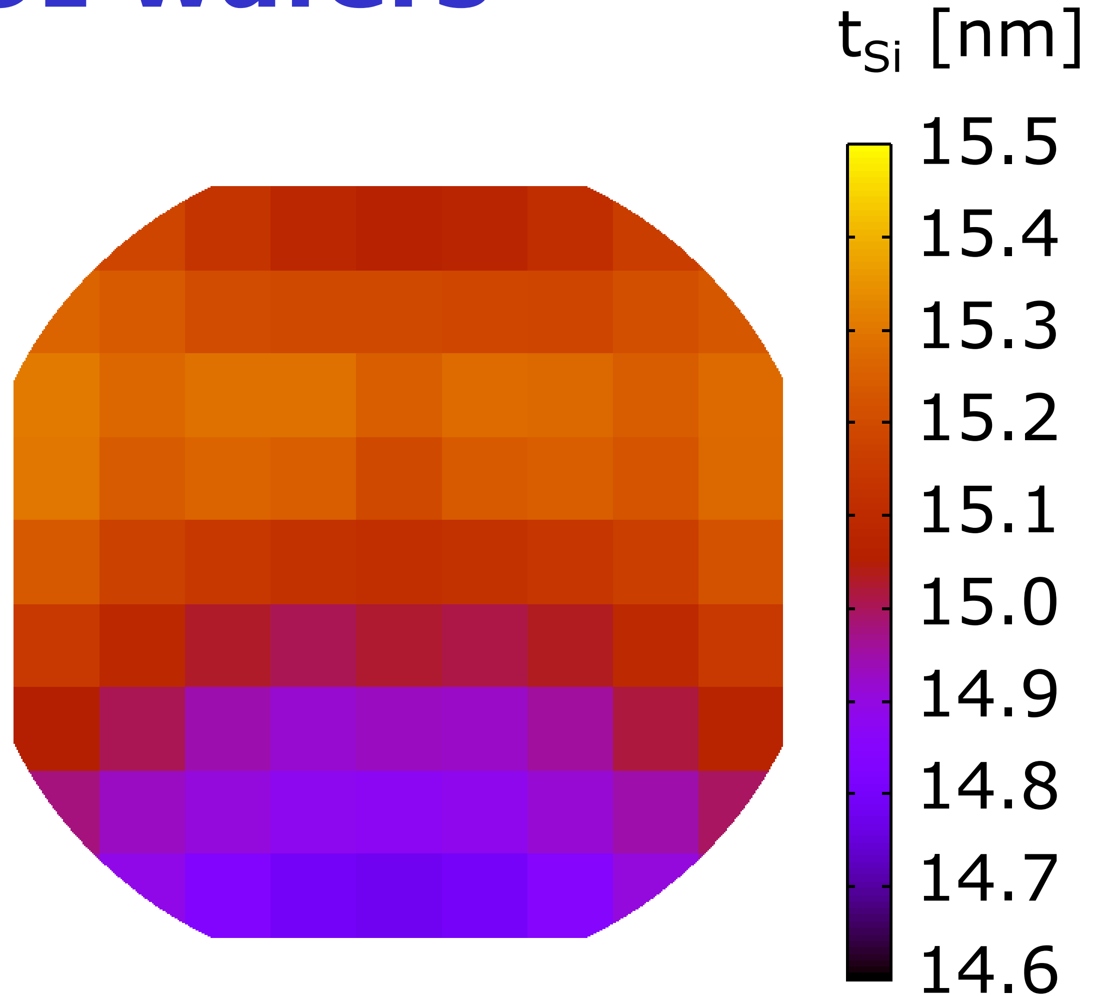
MOSFET Batches

1. Fabrication of sSOI wafers for JPP
2. HKMG, SB-S/D on bulk-Si
3. HKMG, SB-S/D on FD SOI

4. HKMG, SB-S/D on SOI and sSOI
   - 4b. Temperature Budget of HKMG
5. sGe MOSFETs
6. Locally sSi channel (Ge dots) MOSFETs
7. SB-contacts on sSOI (L_{min}=60 nm)

sSOI wafers

- Procedure to reduce wafer size to 100 mm in JPP
- Thinning of Si by oxidation and HF etching
- t_{Si}=15 ± 0.5 nm



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Joint Batch Processing

THE UNIVERSITY OF WARWICK

- sSi or sGe growth
- Layer Transfer, sSOI
- Isolation
- High-k, $LaLuO_3$
- Metal gate, TiN
- Gate definition
- Thin spacers
- DS SB-contacts
- Metallization

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Joint Batch Processing

KTH
VETENSKAP
OCH KONST

KTH Information and
Communication Technology

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HKMG + DS SB S/D

BATCH 2

poly
TiN
$LaLuO_3$
PtSi | PtSi
Si

BATCH 3

poly
TiN
$LaLuO_3$
PtSi | unstrained Si | PtSi
BOX
Si

- L_{min}=0.5 µm
- $LaLuO_3$ on HF last
- $LaLuO_3$ on SiO_2
- $LaLuO_3$ = 6 & 20 nm
  SiO_2 ref = 4.3 nm
- DS SB S/D
- **Completed M17 May 2009**

1. TiN midgap metal gate
2. Dopant segregated SB S/D
   - Working PMOS and NMOSFETs
   - On bulk-Si devices I_{off} increased by I_B
3. Improvements in $LaLuO_3$ needed
   - Gate leakage and reduced CET

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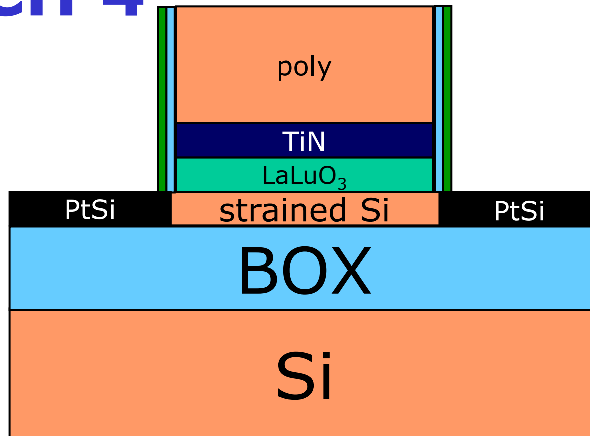
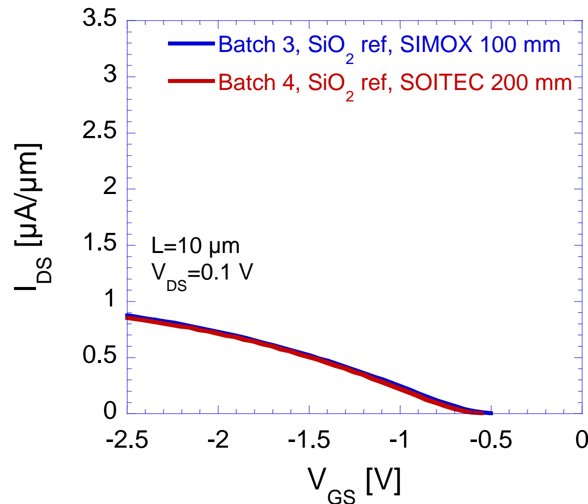
   - 4b. Temperature Budget of HKMG
5. sGe MOSFETs
6. Locally sSi channel (Ge dots) MOSFETs
7. SB-contacts on sSOI (L_{min}=60 nm)

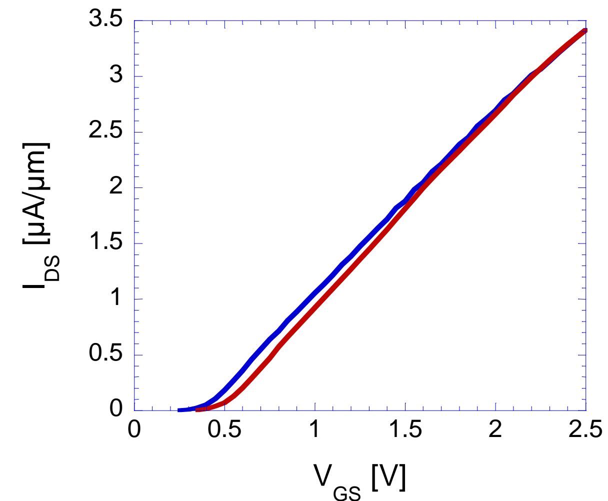
sSOI + HKMG + DS SB S/D

BATCH 4



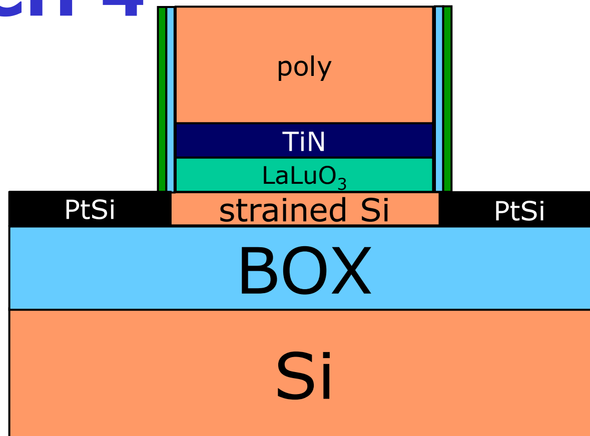
- **Strained SOI** (wafers from batch 1)
  Jülich: t_{Si}=22 nm, stress=1.0 GPa
  SOITEC: t_{Si}=15 nm, stress=1.4 GPa
- **L_{min} reduced to 60 nm**
- **Dopant segregated PtSi SB-contacts**
- **Improved $LaLuO_3$/TiN process module**
  Chemical oxide + $LaLuO_3$ deposition
  MESA isolation improved with spacers
  EOT=0.9 nm and 1.4 nm
- **Completed M29 (May 2010)**





sSOI + HKMG + DS SB S/D

BATCH 4



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Extensive characterization of L=10 µm devices

- CET is 4.4 nm , 2.8 nm and 2.0 nm for SiO_2, 6 nm $LaLuO_3$ and 3 nm $LaLuO_3$
- Gate leakage reduced significantly compare to B2&3
- μ_p and μ_n of unstrained Si and SiO_2 gate oxide is as expected (ref).
- μ_p of unstrained Si and $LaLuO_3$ 90-100 % of SiO_2 reference
- sSOI with 1.0 GPa exhibits increased SS and inferior mobility
- μ_p of 1.4 GPa sSOI and $LaLuO_3$ is the same as unstrained wafers with $LaLuO_3$
- Virtually no NMOSFETs with $LaLuO_3$ is working (measured>600 devices) whereas the SiO_2 ref had 70 % yield of NMOSFETs.

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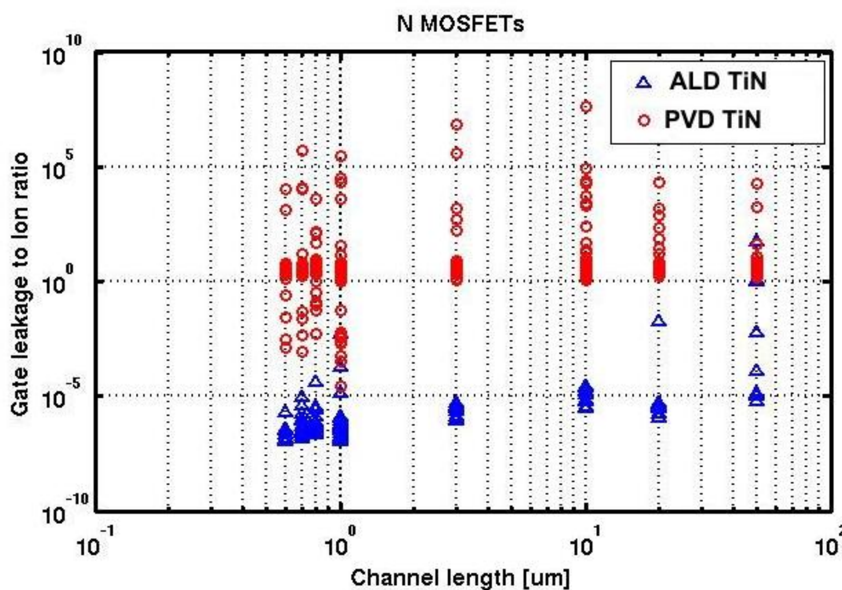
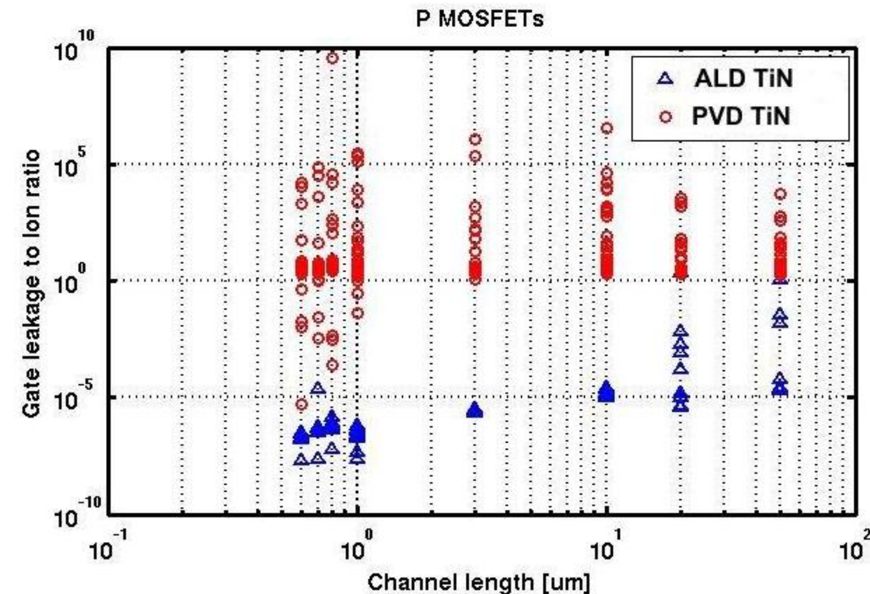
Temperature budget of HKMG

- FP1.3 has shown good mobility of $LaLuO_3$/TiN NMOSFETs using a gate last process (T_{max}=400 °C)
- WP3 developed a gate last process aiming at:
  1. Reproducing the mobility results from FP1.3
  2. Evaluate the temperature budget of $LaLuO_3$/TiN
- High gate leakage after PVD TiN gate
  - Decision to use SiO_2 in B7 and focusing on supporting SB work in WP1





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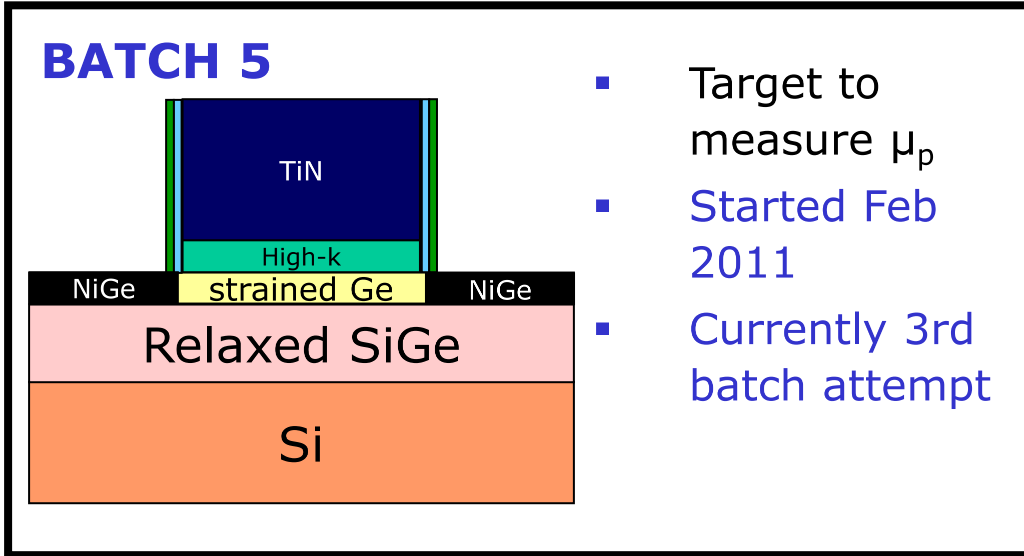
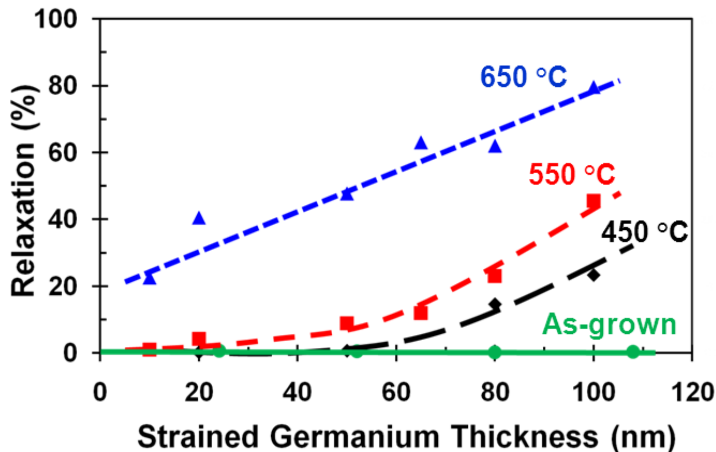
sGe PMOSFETs

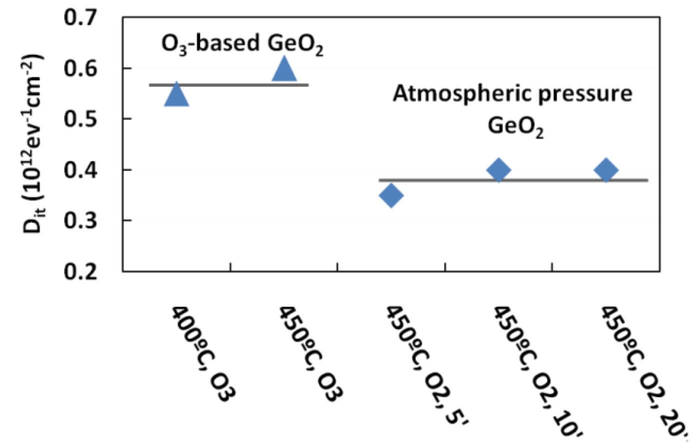


- Surface cleaning of s-Ge and r-Ge
- Deposition/structuring of field oxide
- Atmospheric pressure oxidation forming GeO_2
- ALD of high-*k* dielectric Al_2O_3 and metal gate TiN
- Deposition of a thin cap layer of Si_3N_4
- Structuring of gate contacts using dry etching
- Spacer formation
- Selective wet etch of the high-*k* dielectric
- Formation of NiGe S/D contacts
- Isolation layer of SiO_2/Si_3N_4
- Contact opening and metallization



Investigated gate stacks

1. $LaLuO_3$
2. $Al_2O_3/LaLuO_3$
3. GeO_2/Al_2O_3



sGe PMOSFETs Batch Results

$TiN/Al_2O_3/GeO_2/Ge$

NiGe

Field Oxide

$TiN/Al_2O_3/SiO_2$

$TiN/Al_2O_3/GeO_2/Ge$

NiGe

Field Oxide

$TiN/Al_2O_3/SiO_2$

Si reference devices are working

TiN gate on Ge active regions deteriorated after selective NiGe etch

- Occured on first and second batch attempt
- For 3rd attempt we investigate other selective etchants as well as tailoring of stress in TiN film.
- 3rd attempt completed next week and this work continues beyond NANOSIL

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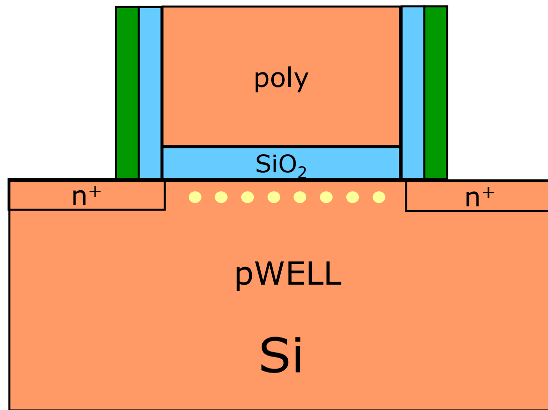
Locally sSi channel MOSFETs

BATCH 6



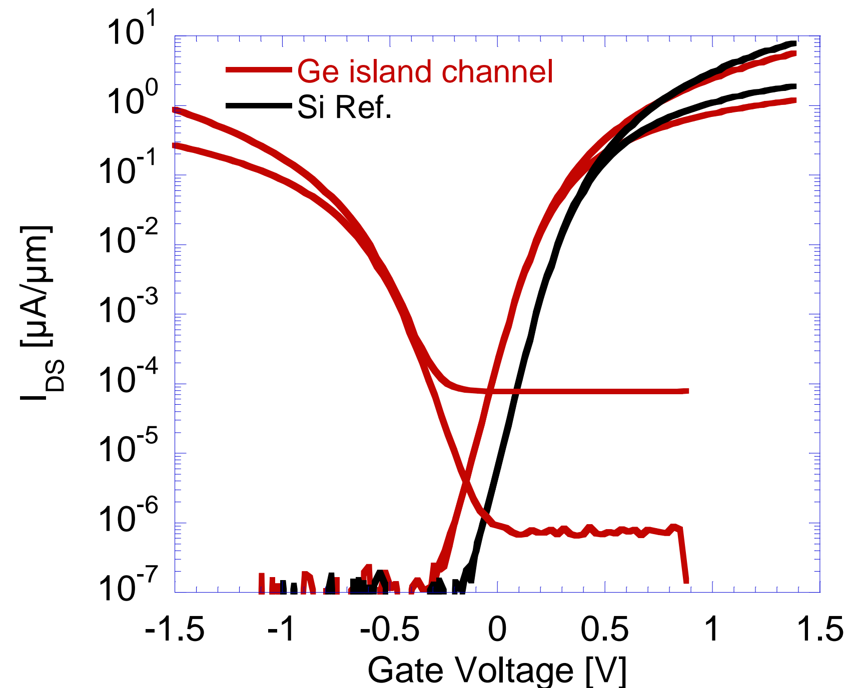
Target:

Influence of small range (5-20nm) strain fields on mobility and V_T in n- and pMOSFETs

Method:

MBE-growth of Ge islands by low growth temperatures. The Ge layer is embedded in an 10 nm undoped Si channel region.

Started Nov 2010 Completed February 2011



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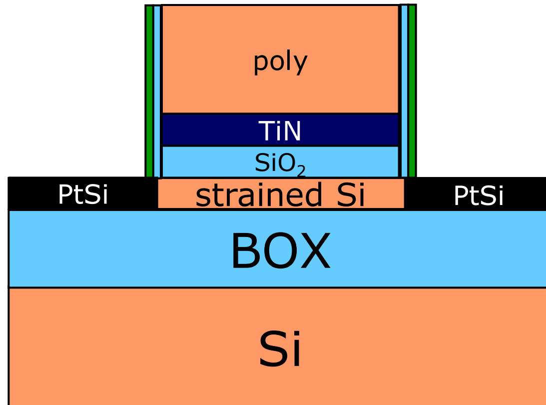
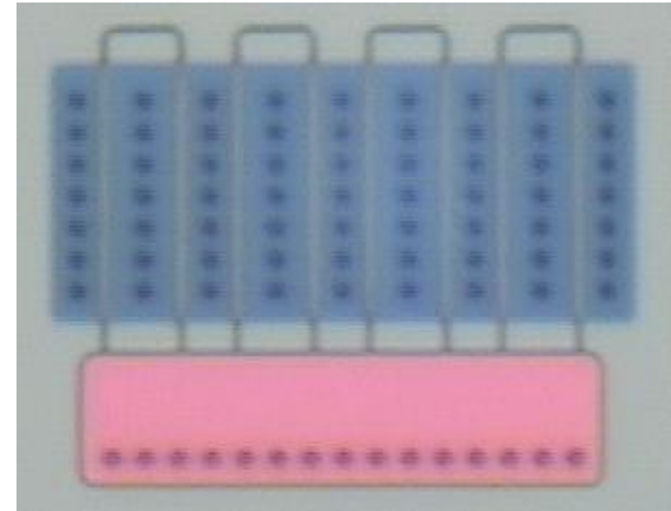
sSOI and DS SB contacts

BATCH 7



- **Strained SOI 1.4 GPa**
  SOITEC: t_{Si}=15 nm
- **L_{min} = 60 nm**
- **Dopant segregated PtSi SB-contacts**
- **Thermal SiO_2/TiN**
- **Started March 2011**
- **Completion next week**



	ϕ_{BP} w/o DS	ϕ_{BP} Boron DS	ϕ_{BN} Arsenic DS
Unstrained SOI	250 meV	125 meV	270 meV
Strained SOI 20%	210 meV		220meV
Strained SOI 40%	183 meV	105meV	160meV

WP3 Summary

1. All deliverables and milestones completed
2. Several process modules integrated in JPP
3. Batch 1-6 completed
4. Batch 7 completed next week
5. Characterization ongoing on B4b, B5, B6

Work beyond NANOSIL

- sSi DS SB contacts
- sGe (NMOS and PMOS)
- Nanowire process used in EU Network of Excellence Nanofunction

Thanks for your attention