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July 2010

**CEA Grenoble (France) - PostDoc Open Position at LETI**

**Duration: 1 ys (+1ys)**

**Position: "Electrical Characterization of Resistive Memory Devices"**

Applicants should have a PhD degree. Candidates with a strong background in microelectronics, electrical measurements are encouraged to apply.

*The LETI environment*

A unique scientific, industrial and cultural environment, With its research centers, university campus, 500 foreign companies and 40,000 scientists, engineers and technicians employed in the area, the Grenoble-Isère region, otherwise known as France's Silicon Valley, mixes world-class intellectual and scientific dynamism with exceptional quality of life. It is the ideal springboard for Leti's expansion.

Located in the heart of a unique scientific, industrial and cultural environment, the CEA-Leti Institute for micro- and nanotechnology research offers researchers alike a rewarding place to work. You will grow in an environment where the scientific community is passionately engaged in technological research: men and women who are ready to share their expertise with you in your scientific and professional development. From technologies to applications, Leti is a world leader in the creation and transfer of innovation within Europe. With 1,400 patents, its intellectual property portfolio is unusually rich for a research institute.

With Minatec, Leti boasts a concentration of resources that is unrivalled in Europe. An international benchmark in micro- and nanotechnology, the Minatec campus is home to state-of-the-art infrastructure and equipment that is available to every researcher working at Leti. Leti's special place in the global research community is partly due to its natural surroundings in the heart of the French Alps, which offer an excellent quality of life. Leading experts who have been attracted to this natural environment have helped Leti form its mutually rewarding industrial alliances that provide students an unmatched learning experience (<http://www-leti.cea.fr/en>).



*The PostDoc Description*

Resistive memories are simple devices based on MIM structures where a dielectric is integrated between metal layers. Up to now, only few works have reported the process integration of these memories in the back-end-of-line and it is always difficult to predict the reliability characteristics of RRAM, since the resistance switching mechanisms are not yet fully understood. On the other hand, nanodevices that implement both logic and memory in the same device would revolutionize circuit and nanoarchitecture implementation and resistive memories based on oxides are seen as one of the most promising candidate for this new challenge.

Different Resistive Random Access Memories (RRAM) technologies can be envisaged for this application and one of the main problems is to find materials with the right properties, compatible with CMOS back-end integration (in term of contamination, thermal budget, ...). RRAM based on binary oxide consisting of a dielectric layer (NiO, TiO<sub>2</sub>, HfO<sub>2</sub>, , ...) between a top and a bottom electrode (usually Pt or TiN) constitute a highly promising solution. An other approach consists to use a soluble electrode (such as Cu) which can reversibly diffuse in a dielectric to form a conducting path.

Main objectives of this postdoc position will be the **electrical characterization** in view of basic **physical modelling** of resistive RAMs memories.

The activity of the postdoc will be focused on electrical characterization of devices with integrated bistable oxides (ie NiO, HfO<sub>2</sub>): mainly he will address both the **hardware & methodology** to address the non-volatile memory performances (ie write/erase, data retention and endurance), and he will perform measurements on several devices featuring different bistable oxides (ie NiO, HfO<sub>2</sub>...). Note that particular attention will be devoted to pulsed measurements tailored for “non-polar” or “bipolar” devices. At the same time he will perform also measurements on blanket wafers of the same bistable oxides in order to possibly devise the properties of soft and hard-breakdown with a direct material inspection.

Once memory performance are understood, he will perform in-depth characterization on particular features (ie conduction mode, failure mechanisms) that can provide a better understanding of the physical mechanism involved during memory operation. Possibly he will extrapolate with simple models the behaviour of such devices to different architectures.

The work will be performed in LETI/D2NT department, in the electrical characterization and simulation laboratory (LSCE) in close collaboration with the material engineering group (L2MA), the specialists of materials characterizations (nanocharacterization platform), with specialists of memory integration from the Laboratory of Advanced Memory Technologies (LTMA).

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