PostDoc Open Position

July 2010

CEA Grenoble (France) - PostDoc Open Position at LETI
Duration: 1 ys (+1ys)

"Electrical Characterization of Phase-Change Non-Volatile Memories"

Applicants should have a PhD degree. Candidates with a strong background in microelectronics, electrical measurements are encouraged to apply. Nice to have: knowledge of phase-change memories.

The LETI environment

A unique scientific, industrial and cultural environment, With its research centers, university campus, 500 foreign companies and 40,000 scientists, engineers and technicians employed in the area, the Grenoble-Isère region, otherwise known as France's Silicon Valley, mixes world-class intellectual and scientific dynamism with exceptional quality of life. It is the ideal springboard for Leti's expansion.

Located in the heart of a unique scientific, industrial and cultural environment, the CEA-Leti Institute for micro- and nanotechnology research offers researchers alike a rewarding place to work. You will grow in an environment where the scientific community is passionately engaged in technological research: men and women who are ready to share their expertise with you in your scientific and professional development. From technologies to applications, Leti is a world leader in the creation and transfer of innovation within Europe. With 1,400 patents, its intellectual property portfolio is unusually rich for a research institute.
With Minatec, Leti boasts a concentration of resources that is unrivalled in Europe. An international benchmark in micro- and nanotechnology, the Minatec campus is home to state-of-the-art infrastructure and equipment that is available to every researcher working at Leti. Leti's special place in the global research community is partly due to its natural surroundings in the heart of the French Alps, which offer an excellent quality of life. Leading experts who have been attracted to this natural environment have helped Leti form its mutually rewarding industrial alliances that provide students an unmatched learning experience (***http://www-leti.cea.fr/en*)*.**

The PostDoc Description

In an effort to overcome the scaling limit of the floating gate non-volatile memory (NVM) technology below the 30nm design rule, the semiconductor industry has been forced to find alternative NVM. Phase change random access memory (PCRAM or PCM) attracts great interest not only because it satisfies the various demands for NVM devices but also because its fabrication process is relatively simple.

For the digital data storage PCRAM uses the reversible phase change between the crystalline and amorphous state of chalcogenide materials, such as $Ge_2Sb_2Te_5$ (GST), by joule heating. The crystalline GST has a low resistivity and the amorphous GST has a high resistivity, which corresponds to the data

"0" (crystalline) and data "1" (amorphous). In PCRAM cells the reversible switching between these two states can be achieved by applying a short (~ 50ns) and high current pulse for the transition from the crystalline to the amorphous state (reset process) and a relatively long (I_{set} ~ 100ns) and low current pulse for switching from the amorphous to the crystalline state (set process). Recently, there have been great advances in PCRAM development, but several reliability issues still remain to be solved before PCRAM will become a reliable commercial product. One of the main issues is the data retention at high temperature and the high level of I_{res} has been the major obstacle for further scaling of PCRAM because of the limited on-current drive capability of the cell transistor (< 1mA/µm).

To address these issues, a big effort in different research topics is still needed, as the evaluation of new phase change materials (GST, SbTe, GeSb, GeTe...), process technology innovations (PVD, CVD, ...), engineering of various device structures (planar Phase Change Bridge cell and vertical pillar or µ-trench cells), and device designs. This topic is targeted at LETI/MINATEC with our nanotechnology facilities.

Main objectives of this postdoc position will be the **electrical characterization** in view of basic **physical modelling** of chalcogenide materials and integrated devices for application to sub-45nm embedded Phase-Change Non-Volatile Memories.

Electrical characterization (program dynamics, data-retention at different temperature, cycling, data-retention after cycling, disturb during cell reading and programming of nearby cells...) on test structures will be performed in order to put in evidence the main performances and degradation modes. Electrical characterization on blanket deposition will be operated as well, in order to assess the chalcogenide resistivity, crystallization temperature and thermal conductivity.

The postdoc will be involved in a detailed experimental work, but he will have also to face the theoretical principles governing the functionality of a Phase-Change Memory. In particular, the obtained experimental data will be coupled to a basic **physical modeling** of the chalcogenide materials integrated in the test structure, considering the electrical & thermal dynamics governing the phase change process of PCRAM devices.

The final intent is to improve the test methodology suitable for phase-change memories, perform a systematic characterization of different test devices in order to understand the most important parameters that govern the electrical behaviour of PCRAM cells and include them into very simple models that can be integrated in spice-like simulations to simulate the electrical behaviour of arrays of cells.

The postdoc will interact in strict correlation with the material engineering group and device team to obtain properly tailored chalcogenide materials **integrated in test device structures.**

L. Perniola
17, rue des Martyrs, 38054 Grenoble
Tel. : 04.38.78.10.72,
Fax. : 04.38.78.51.40
e-mail : luca.perniola@cea.fr

V.Sousa / J.F.Nodin
17, rue des Martyrs, 38054 Grenoble
Tel. : 04.38.78.43.07/04.38.78.98.28
e-mail : veronique.sousa@cea.fr
jean-francois.nodin@cea.fr