Fundamental study of the short channel carrier mobility degradation and of the impact of realistic non uniform strain fields on the electrical performances of the FDSOI technology for advanced technological nodes (< 20nm)

Summary

In order to boost the performance of the CMOS technology (*Complementary Metal Oxide Semiconductor*), the ultra-thin film *Fully Depleted Silicon On Insulator* (FDSOI) architecture is a good candidate as an alternative to the classical MOSFET. The electrostatic interest of this architecture is now well known and the implementation of this technology in industrial fabs. is on-going.
Nevertheless, this technology has still to demonstrate that the gain of performance, compared to the traditional CMOS technology, for advanced technological nodes (14nm & 11nm) is maintained. This step requires calibrated and predictive TCAD (*Technology Computer Aided Design*) simulations to build a meaningful compact model and then to be able to evaluate the technology at integrated circuit level.
The up-to-date experimental results obtained on the FDSOI MOSFET demonstrate a degraded mobility for both electrons and holes for the smallest gate lengths. This mobility degradation is also observed for the traditional bulk technology but is not still well understood. No consensus can be found in the literature on the physical phenomenon which can cause this degradation of mobility (interaction with charge-free defects, quasi-ballistic transport, source and drain junction impact, etc.). Nevertheless, it seems to appear that this mobility degradation cannot be physically reproduced in the standard TCAD tools due to an intrinsic limitation of the drift-diffusion and Hydrodynamics approaches which are classically available in commercial simulation tools (C. Jungemann *et al.*, IEEE Trans. Electron Dev. 52 (2005), 9383).

The understanding of the physical phenomena which degrade the carrier mobility is now mandatory to be able to evaluate the performances of sub-20nm devices with a good confidence on the predictions of the simulations. This better understanding relies on a good description of the interaction mechanisms and a meaningful extraction of the effective mobility fort short channel devices in order to be able to correct the TCAD tools in order to make it as predictive as possible for the advanced CMOS technology nodes.

Moreover, the observed degradation of mobility requires the use of mobility “booster” process options like strained materials which, at first order, induced a mobility enhancement due to the piezoresitive properties of silicon. Therefore we have to handle the realistic strain field in a TCAD environment to evaluate the impact of the strain engineering options on the electrical characteristics of the FDSOI devices. The impact of non-uniform realistic strain field can be evaluated through the use of a 3D quantum transport code developed at CEA (NEGF approach).

Main Objectives of the proposed PhD thesis period:

- From an experimental data base available at CEA-Léti (undoped strained & unstrained FDSOI devices and highly doped strained & unstrained bulk devices), the candidate will have to extract the impact of the different phenomena which can degrade or boost the mobility by studying the impact of the gate length reduction as a function of the temperature. The reviewing of the mobility extraction procedure will be necessary to propose the most pertinent mobility measurement for short channel devices ;
- The candidate will have to review the main mechanisms causing short channel mobility degradation through the use of a Monte-Carlo (MC) code developed at IEF (*Institut d’Electronique Fondamentale*) to perform effective mobility calculations ;
- The development of an analytical and physical model which can reproduce the short channel mobility degradation will then be necessary in order to implement this physical correction in the TCAD simulation environment and make it predictive for advanced technological nodes ;
- Based on a collaborative work on both quantum transport NEGF and MC studies, the impact on the electrical performances of realistic non-uniform strain field in the TCAD environment will be evaluated ;

- Finally, the predictive TCAD simulation tool will be included in an extraction flow in order to provide the parameters needed at the compact model level and to make predictive the evaluation of the FDSOI technology at integrated circuit level for advanced technological nodes.

The LETI is one of the leading research institute in the field of thin film CMOS technology. The PhD thesis will take place in CEA-Léti (Grenoble, France) in the Simulation and Compact Modelling laboratory of the NanoTechnology division. This work will be performed in close collaboration with the Institute of Fundamental electronics in (Orsay, France (near Paris)) and will need a large ability of the candidate to work in close relationship with the team of electrical characterization as well as the technology developers.

Needed Background

Physics of semiconductor materials

In Practice

Date of beginning: 01/10/2011
Location:
CEA-Léti, Grenoble (France)
Nanotechnology Division
Simulation and compact modelling laboratory
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