



-NANOSIL NoE-FP7 -
Review Meeting, Stockholm, May 26, 2011

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Grant agreement n° 216171

Title: Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications

Agenda of the Review Meeting

- 9:00 – 9:35 General NANOSIL presentation
- 9:35 – 10:10 WP1
- 10:10 – 10:45 WP2
- 10:45 – 11:20 WP3
- 11:20 – 11:55 WP4
- Lunch-*
- 13:30 – 14:05 WP5
- 14:05 – 14:40 WP6
- 14:40 Private discussion between the Project Officer and the Reviewers
- 15:30 Feedback from the Project Officer and the Reviewers
- 16:00 End of the meeting *and visit of KTH facilities*



-NANOSIL NoE-FP7 -



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NANOSIL Objectives (1)



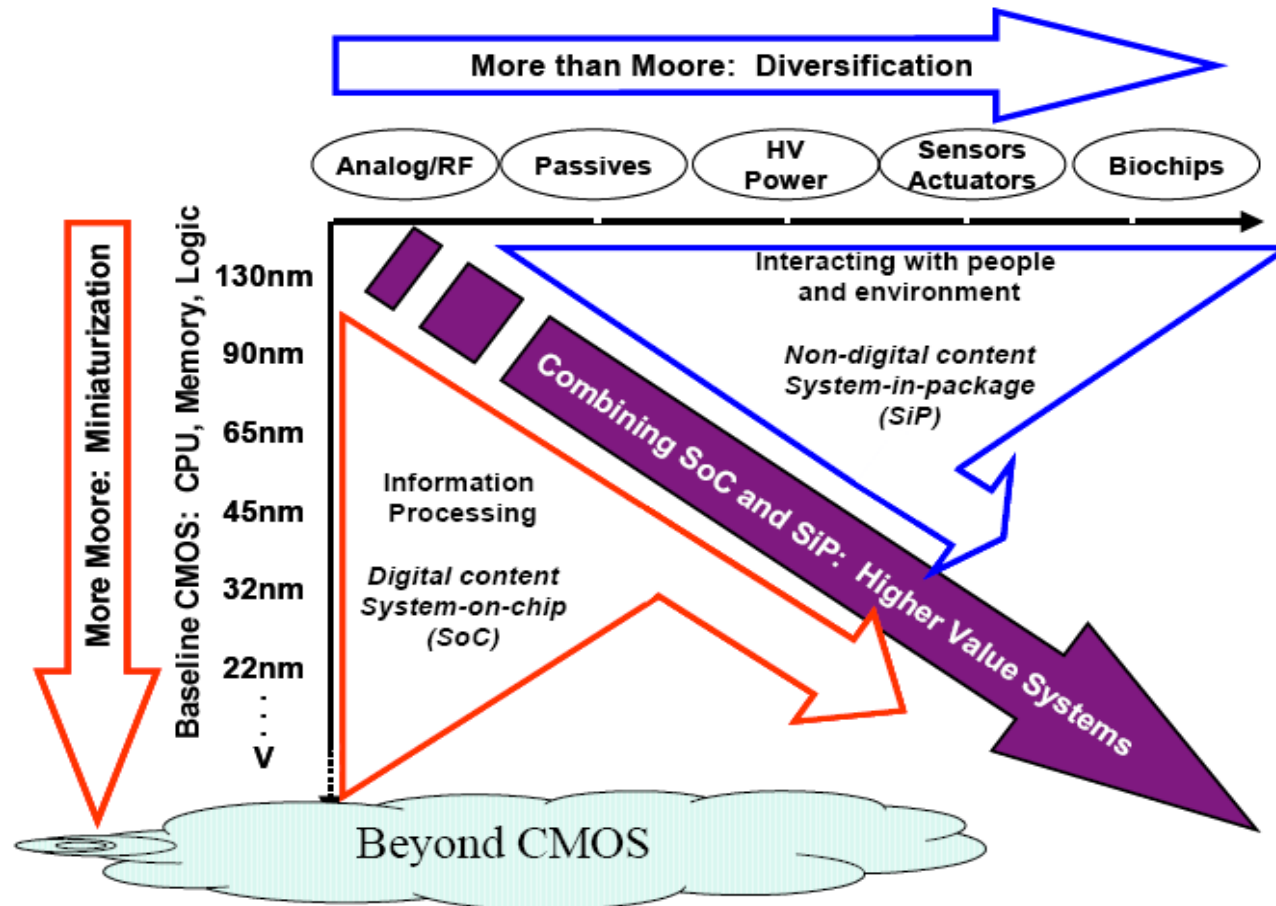
- ⇒ 28 Partners from 11 European countries:
 - main European Labs, Research Centres in this field
- ⇒ Push the limits of Si integration down to nanometric dimension
- ⇒ Work on N+4 technology node and beyond for:
 - studying and validating new concepts, novel materials and technologies, innovative device architectures using joint platforms
 - identifying the most promising topics for future information and communication technologies and updating roadmaps
- ⇒ Overcome the number of research challenges of ultimate CMOS and beyond-CMOS nanodevices in order to speed up technological innovation for the Nanoelectronics of the next 2-3 decades
- ⇒ Allow **integration of Si-based innovative CMOS and emerging non-CMOS** devices on one Si chip, which is a strategic issue for the next IC generations



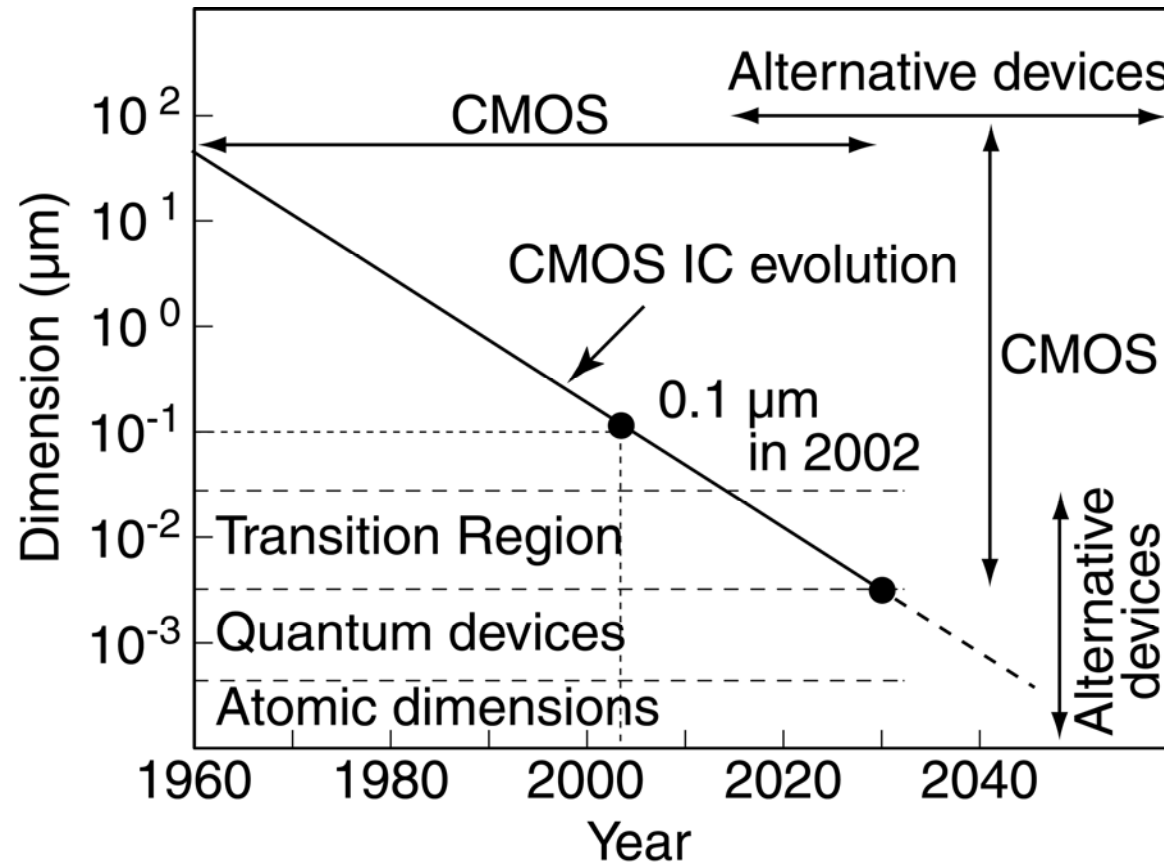
NANOSIL Objectives (2)

- ⇒ Perform training and dissemination activities, organize Conferences and Workshops in order to develop high competence levels in Europe
- ⇒ Strengthen interaction between the Scientific Community and the European Industry
- ⇒ Establish close links with other European and National projects in order to enhance the overall efficiency of the European research in Nanoelectronics
- ⇒ NANOSIL acts as a cluster of projects, existing at the beginning or new ones to be proposed, providing they are sufficiently forward-looking
- ⇒ Prepare the path for future industrial applications in the field of communications, computing, consumer electronics, health, environment.

Nanoelectronics Landscape



IC evolution in the next decades



=> 2010: 45nm -----> 2025: 8nm

Roadmap: Ultimate CMOS Logic & Memories



- **Short term ITRS ≥ 2014 (19nm/Flash - 25nm/DRAM-MPU)**

- CMOS:** 2nd gener. high k/metal ; Si+stress ; S-D engineering ; FD-SOI ; Variability/Reliability/Transport mechanisms
- DRAM:** high k/Capa. + low leakage access Tr./Capa.; capacitor-less
- NVM:** scalability of tunnel/interpoly dielectric-high k ; multiple bit/cell

- **Medium term ITRS $\approx 2017-2020$ (14-18/11-13 nm)**

- CMOS:** Nth gener. high k/metal ($k > 30$) – EOT $< 0.7/0.8$ nm ; Strained Si or altern. Channel on Si/Ge-III-V ; Advanced S-D architectures ; FD-SOI or Multi-gate bulk/SOI ; V_{dd} scaling, Variability/Reliability/Transport/Short channel-leakage model. and charact.
First principle simulation/quantum/MSB MC simulations ; Modeling of chemical, thermomechanical and electrical properties of new materials
- DRAM:** scaling capa./high $k > 60$; capacitor-less
- DRAM & SRAM:** replacement solutions (3D, ...)
- NVM:** density and voltage scaling/3D integration/ non-charge storage: PCRAM, RRAM...
with diode selectors

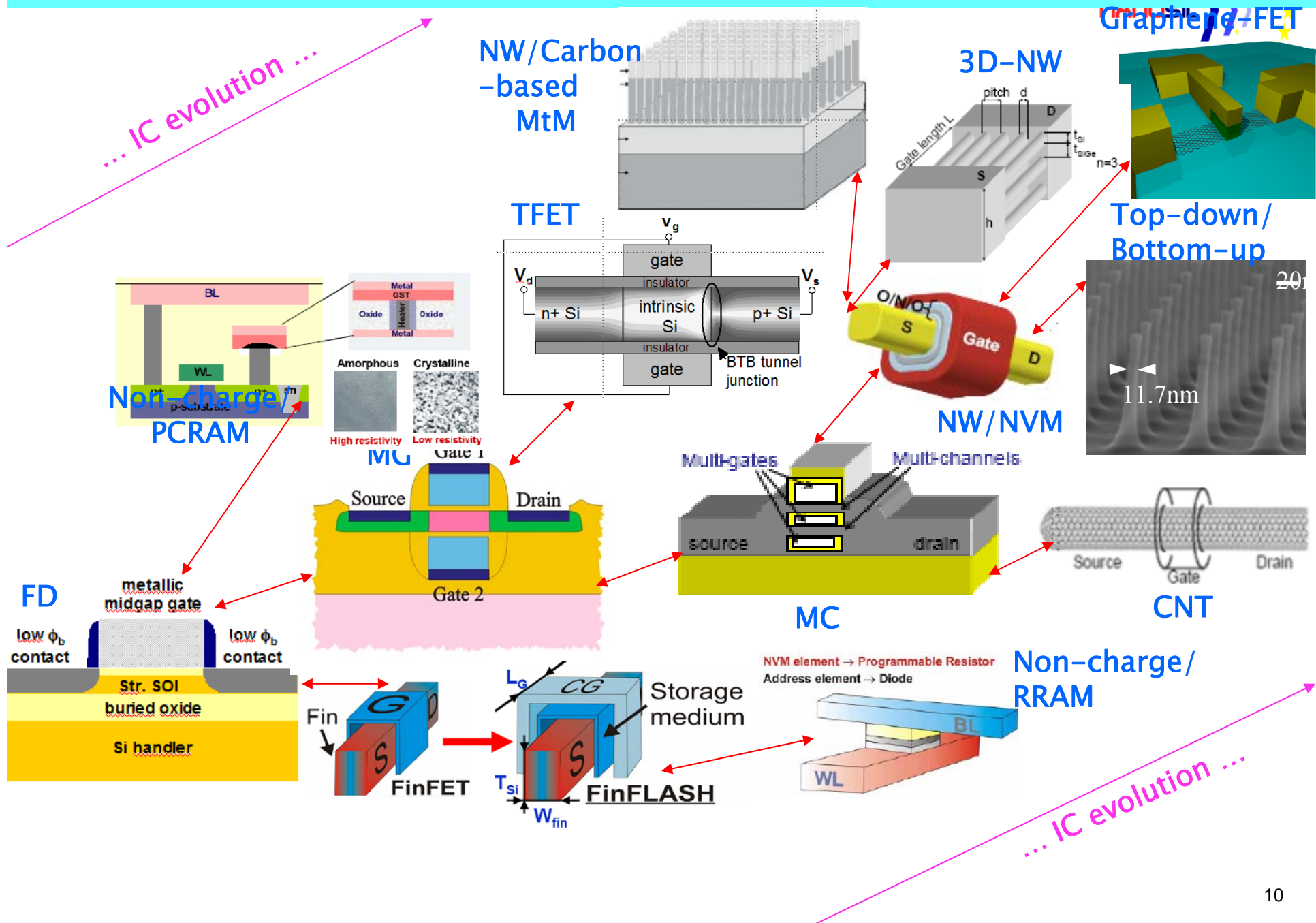
- **End ITRS ≥ 2025 (8nm: *end of scaling?*)**

- CMOS:** top-down Si or Ge/III-V 3D nanowires on Si-CMOS platform
- (Universal/embedded) **Memories:** replacement solution:
(3D, Nanowires, non-charge storage with NW selector)

Roadmap: Beyond-CMOS (300K, CMOS compatible, Ultra Low Power)

- **Beyond-CMOS:** new devices/technologies/alternative state variable: spintronics, molecular electronics, carbon electronics, nanowire electronics, NEMS switches, direct self-assembly, etc.
- **Medium/Long term: New information processing and memory technologies to replace CMOS:**
 - Small slope switches: TFET/IMOS/Fe-gate... (including ultra-thin film, Si/Ge/III-V, multi-gate, carbon-based)
 - Spin transfer torque (STT) MRAM / Racetrack memory
 - Variability/Reliability/Transport/Defects modeling/simulation and characterization
- **Long term:**
 - Carbon-based (Graphene, CNT) FETs nanoelectronics with:
 - * high on-off ratio co-integrated with high κ dielectric and low resistance contacts
 - * Control of CNT properties, bandgap distribution and metallic fraction
 - SpinFETs
- **Very Long term:**
 - Controlled assembly of nanostructures (or combining top-down and bottom-up process.), such as CNTs or nanowires, in precise locations for devices, interconnects
 - Ferroelectric-gate FET memory, nanoelectromechanical RAM, nanowire phase change memory, molecular memory.

Nanoscale FET roadmap



Strategy for the European Research in Nanoelectronics NANOSIL



=> Long term (N+4 and beyond):

NANOSIL

Scientific approach/ long-term research based on the competences of the scientific community

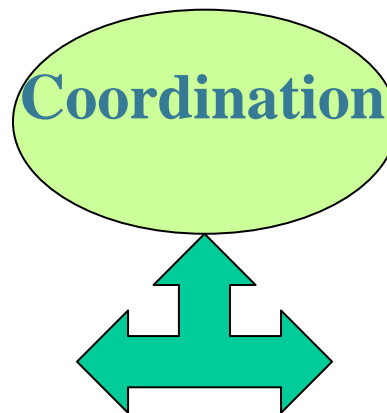
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Network of flexible research infrastructures

=> Rapid test and validation of new concepts, techniques, materials, technologies and very innovating devices; detailed understanding

Medium term (N+2/3)

Pre-industrial research and platforms



Short term (N, N+1)

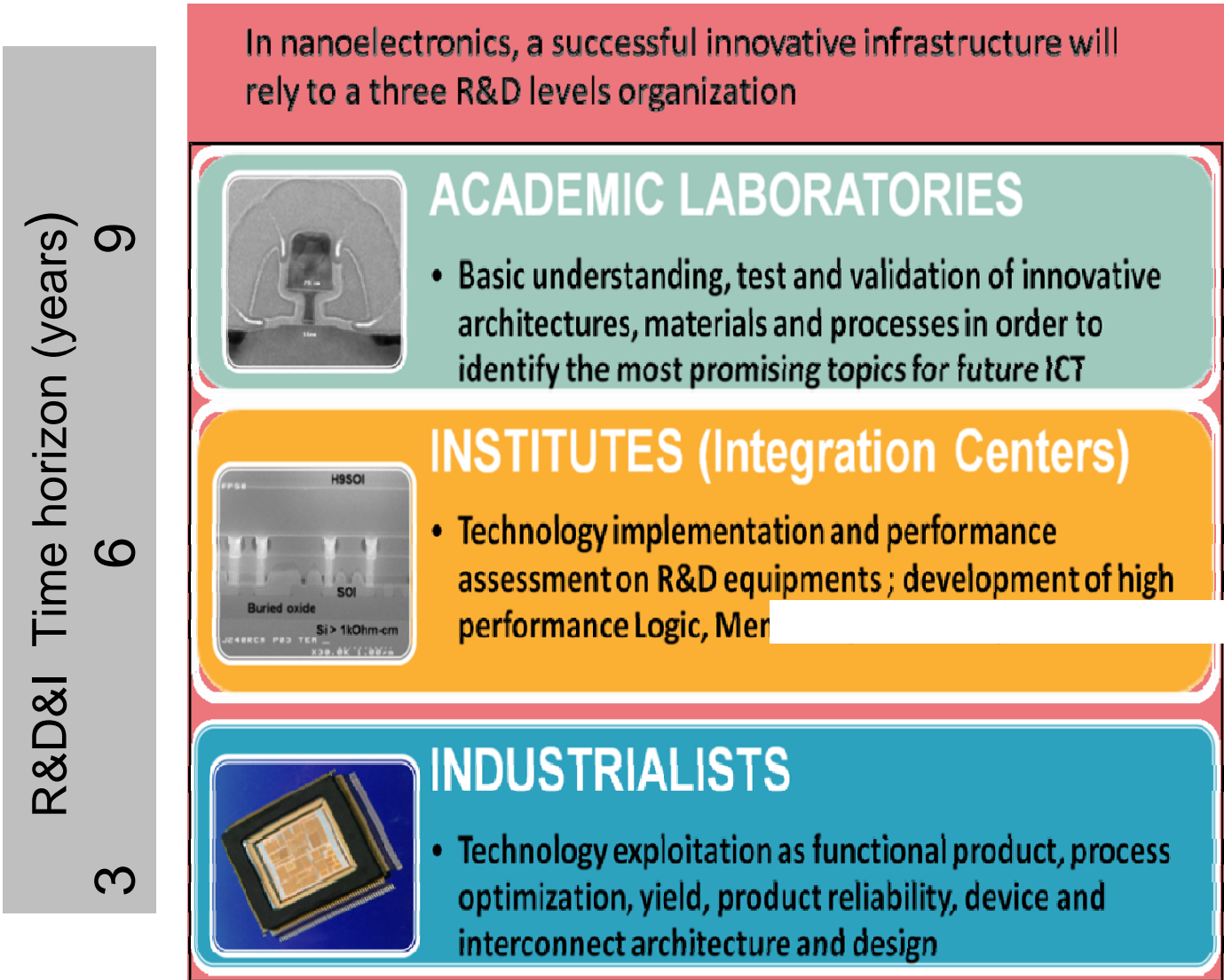
Industrial approach for the development of new technologies

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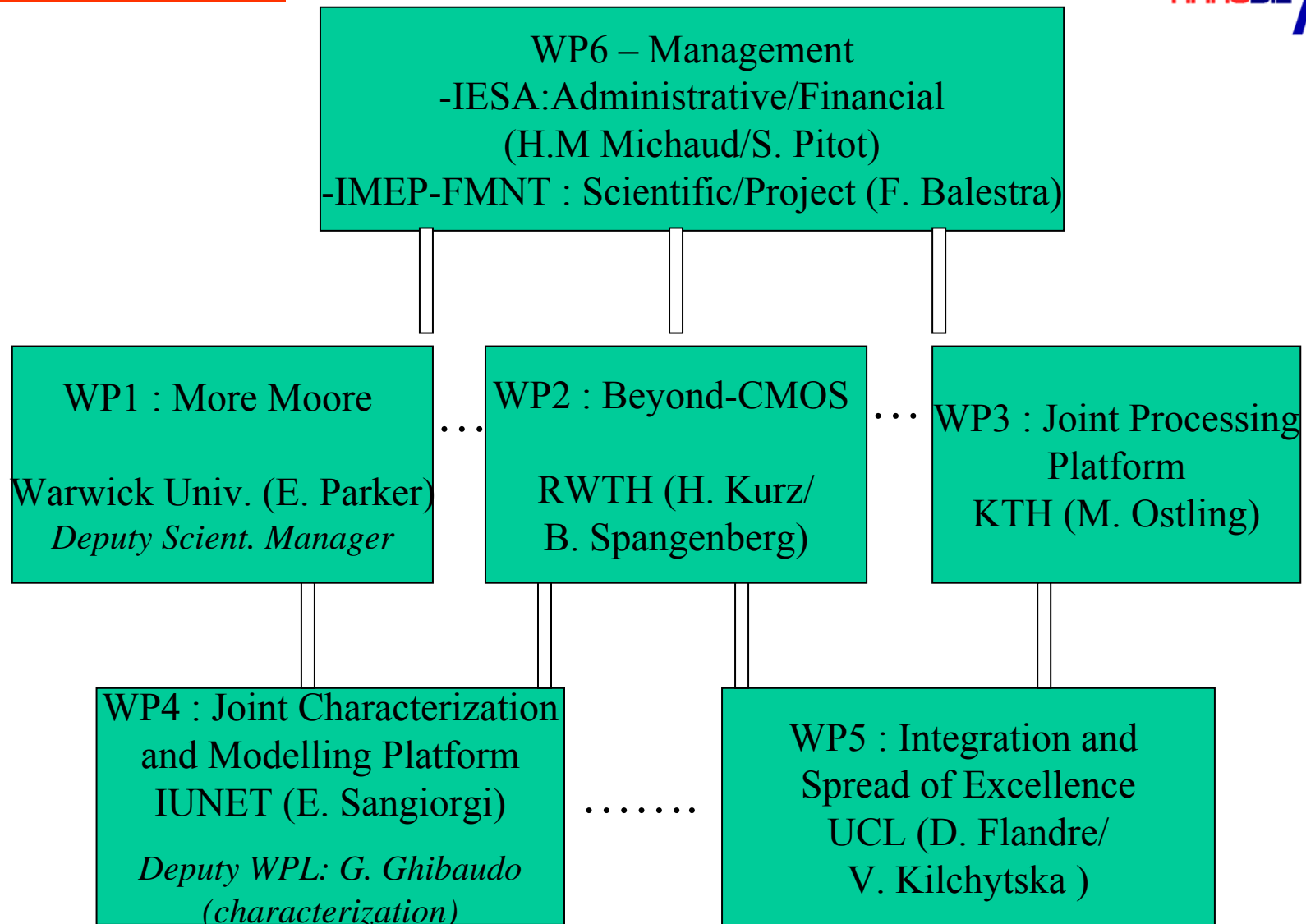
Industrial platforms



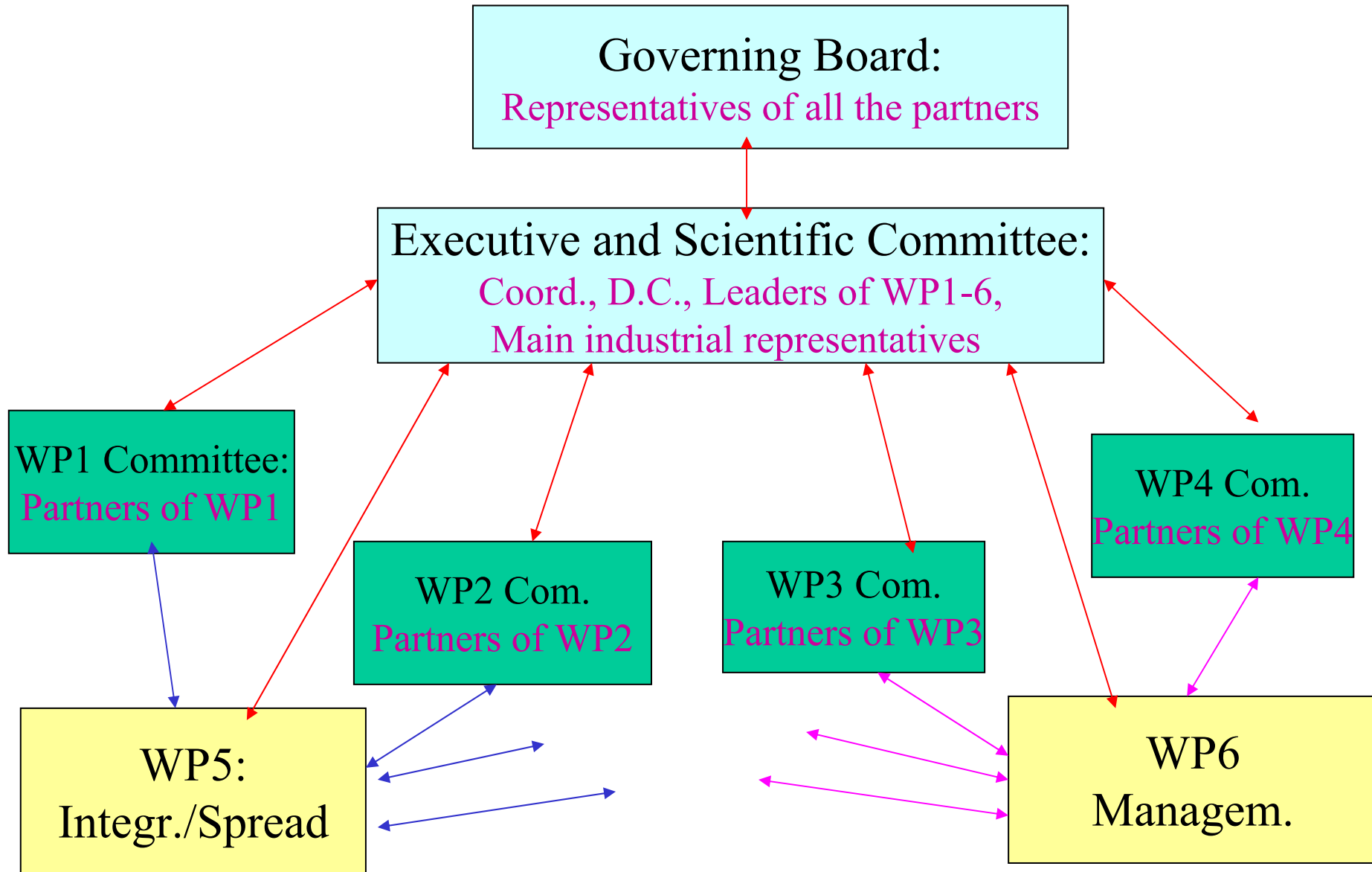
eni² 's ambition: being a 2 way bridge between academic and Industrialists to help the KET's mission to succeed



NANOSIL WPs



Robust organisational, management and governance structure :



NANOSIL projects

- *More Moore:*

- FP1.1 (*S. Mantl*): Appraisal of **new channel materials** for end of CMOS era
=> sSOI, sSiGeOI and sGeOI, various channel orientations, etc.
- FP1.2 (*E. Dubois*): Routes to realisation of **very low Schottky barrier contacts** for end of CMOS era
=> cover a wide spectrum of silicide materials and dopants for the realization of dopant-segregated metallic junction ; integration of such junctions on strained and unstrained layers on insulator
- FP1.3 (*O. Engstrom*): Identification and appraisal of **novel gate stack materials/combinations** for end of CMOS era
=> $k \cdot \Delta E > 70$

NANOSIL projects (2)

- *Beyond CMOS:*

- * FP2.1 (*J.P. Raskin*): Evaluation of the prospects of **1D nanowires** for the post-CMOS era
 - => with strain, low Schottky barrier contacts, high k/metal gate stacks, parallel nanowires
- * FP/AS2.2 (*M. Baus/D. Neumaier*): Investigation of the prospects for **carbon structures - especially graphene**, and their technological potential
- * FP2.3 (*A. Ionescu*): Assessment of the performance of **new nanoelectronic switches**:
 - => *impact ionisation (IMOS), tunnelling devices (TFET, RTD), NEM-FET* in order to determine if they can form the basis of new MOS device functionality with very low subthreshold swing
- * FP2.4 (*E. Kasper*): Investigation of routes for producing high densities ($> 10^{12}\text{cm}^{-2}$) of **nanodevices (nanodots, nanowires)** by **templated self-assembly**, and assessment of their technological potential

NANOSIL projects (3)

- ***Visionary projects:***

=> *discussion Forums, brainstorming activities and Workshops* in More Moore (WP1, R. Clerc) and Beyond-CMOS (WP2, B. Spangenberg) areas to **generate new ideas** and identify the **most promising topics** for future information technology

- ***Joint Processing Platform:***

- * *Execute* batch processing for the flagship projects
- * *Coordinate* processing involving several partners
- * *Fabricate* MOSFETs and test structures for the Joint Characterization and Modelling Platform
- * *Strengthening projects* for the development and integration of new processes especially needed by the flagship projects

NANOSIL projects (4)

- *Joint Characterization and Modelling Platform:*
 - * *Integration and validation* of the modelling approaches and tools against ad-hoc, well-characterized template devices
 - * *Design* the test structures to be fabricated in the joint processing platform of WP3 for the implementation of characterization experiments aimed at the calibration of the modelling tools.
 - * *Bring together* the most promising characterization techniques and modelling tools and methods to tackle the main device physical challenges
 - * *Strengthening projects* for the tuning and validation of modelling and characterization techniques to be exploited in the frame of the Flagship Projects

Results



- ⇒ Achievements of excellent results, showing *significant improvements* over the state-of-the-art, in the joint NANOSIL projects combining *process, modeling and characterization activities*
- ⇒ A lot of **exploitable knowledge** has been produced in the field of new materials, processes and devices, characterization methods as well as modelling tools
- ⇒ Many **integration and spreading of excellence** activities
- ⇒ **17 Deliverables** have been delivered in 2010/beginning of 2011
- ⇒ **Strong interaction** between European projects, European-National projects, industrial and scientific communities
- ⇒ Will strengthen the **European structuring** and allow to **speed up technological innovation** for the Nanoelectronics of the next 2 decades

Integration and cooperation



- Close links with other European Projects (STREP GRAND, EUROSIO+ Thematic Network, STREP DUALOGIC, STREP NEMSIC, Compact Modelling Network COMON, STREP SQWIRE, STREP STEEPER, NoE NANOFUNCTION, etc.), ENIAC (SCC management team, WGs), AENEAS and National projects in the same fields
=> enhancement of the overall efficiency of the European Research in Nanoelectronics
- Strengthening of the interaction between the Scientific Community and the European Industry (representatives of the European industry in the E&S Committee, industrial monitors for FPs, joint PhDs and Workshops, joint publications, etc.)
- Many Nanosil Partners and Sinano Institute Members have contributed to the “Sinano Institute vision”, driven by the European Academic Community, to determine the most promising research topics in the MM, MtM and Beyond CMOS Nanoelectronic domains
- Sinano and Nanosil Partners are in charge to establish in 2011 an updated version of the ENIAC SRA concerning the Beyond-CMOS field

Integration and cooperation



-Strengthening of the durable integration:

=> **Seven new Partners** (2009-11) became Members of the Sinano Institute (legal entity created in 2008 for the coordination of the European Academic Community working in the field of Nanoelectronics) :

Tyndall-Cork, Uppsala University, ICN-Barcelona, VTT-Helsinki, Twente University, IES-Montpellier University, IMS Demokritos-Athens

=> **Joint Processing, Joint Characterization and Modelling Platforms**, developed and used in the framework of Nanosil for joint research activities, now **integrated as open Research Infrastructures in the Sinano Institute** (can be used by the European Academic Community, SMEs and Industry)

=> Nanosil Partners and Sinano Institute Members strongly associated to the new initiative launched in 2010 by ST “**ENI2**” (**European Nanoelectronics Infrastructure for Innovation**): coordination of the three levels of R&D activities needed in the nanoelectronics domain:

-**1st level** coordinated by the Academic Community (**Sinano Institute**): long term researches (basic understanding, test and validation of innovative materials, processes and architectures in order to identify the most promising topics for future ICT)

-2nd level: Research Institutes (LETI, IMEC, FhG)

-3rd level: Industry

=> New FP7 **NoE Nanofunction**, devoted to Beyond-CMOS nanodevices for adding functionalities to CMOS in the More than Moore domain (use of Nanosil results)

=> **FET Flagship “Guardian Angels”** for future autonomous ultra low power systems

Response to the recommendations of the second Review Report



All the recommendations of the second Nanosil Review Report have been taken into account. In particular, the following actions have been carried out:

- **Recommendation 1**
- *Deliverables D1.5 and D2.5 do not contain enough (or in some cases any) critical analysis of the trends, prospects and suggested priorities for European R&D and industrial developments in the areas covered by the meetings. A reworking and resubmission of D1.5 and D2.5 to include these missing elements is therefore recommended.*
- The Deliverable **D1.5** (the More Moore Forum report form Year 2) was resubmitted with the required elements, and they are included in D1.10 (the 3rd year Forum report).
- The Deliverable **D2.5** was resubmitted with the required elements

Response to the recommendations of the second Review Report



□ • **Recommendation 2**

- *There have been significant developments in the area of 3D electronic device design and 3D integration since the start of the Nanosil project. The impact, if any, of such developments on the Nanosil N+4 philosophy should be assessed. It is therefore recommended that the consortium consider holding a forum/workshop, or part of a forum/workshop on this topic.*
- A **Workshop** entitled "On the convergence between More Moore, More than Moore and beyond-CMOS", including **talks on 3D integration**, has been organized during ESSDERC-ESSCIRC'2010 in Seville, Spain:
 - Sywert Brongersma, IMEC, Belgium, "CMOS, CMORE, and what to use it for"
 - Peter Baumgartner, Infineon Technologies, Germany, "Scaling Challenges for complex SOC products"
 - Jan Hoentschel, Global Foundries, Germany, "Diversification of Moore's law and its advanced technologies"

Response to the recommendations of the second Review Report



- **Recommendation 3**

- *Several new FP7 projects have recently started, or are under negotiation, in areas related to Nanosil. Two examples include the 'Concept Graphene' and 'Steeper', but there are no doubt others. The consortium is recommended to keep a close contact with the project officer to identify which projects might benefit from links with Nanosil, and to establish such links where feasible. Indeed, in the graphene area we recommend that the main focus of Nanosil should be establishing such contacts with new and existing projects, rather than performing any 'direct' technical efforts on graphene within Nanosil itself.*
- Close contacts have been established **between Nanosil and new FP7 projects** (SQWIRE, STEEPER, CONCEPT GRAPHENE, NANOFUNCTION, etc.). In the **field of graphene**, many contacts have been established with several projects, which was the main activity in this field during year 3 of Nanosil. A **joint workshop** was organized on Carbon-based electronics (14th July 2010 in Aachen, organized by AMO). This yielded in the preparation of one deliverable report and one milestone report: D2.13 (M36) "State-of-the-Art report for Carbon electronics" and milestone-report (M32) on the "EuroCarbon-Workshop".

Response to the recommendations of the second Review Report



- **Recommendation 4**
- *In WP4 the partners should use appropriate figures of merit for device operation, and not concentrate overly on carrier mobility as a means of comparison of likely performance.*
- In order to address the Reviewers recommendation according to which the partners of WP4 should use appropriate figures of merit for device operation, the deliverable **D4.6** on the bechmarking between full quantum and semi-classical transport models was focused primarily on the comparison of complete I_{DS} versus V_{GS} and V_{DS} curves and also on the **cutoff frequency** that are very relevant for RF applications.

Response to the recommendations of the second Review Report



□ • **Recommendation 5**

- *Within the project three more batches of devices are planned to be completed, which means there is a tight schedule in the remainder of the project. In particular batch 7 is due to be processed between M33 and M36, right at the very end of the project. The consortium is recommended to expend all possible efforts to ensure completion of this batch before the final review.*
- As recommended by the reviewer full focus and all resources within WP3 has been allocated to finalize the last batches within NANOSIL. The Ge stressor material was grown and partners decided to proceed to finalize the batch with embedded Ge stressors in the channel.

Response to the recommendations of the second Review Report



□ • **Recommendation 6**

- *It is recommended that future experimental work on templated self-organisation - in WP2, FP2.4 - should focus on Si nanostructures, rather than on the SiGe QDs; indeed, this latter work could be stopped.*
- The growth of **Ge QD wafers was finished by April 2010**. The further activities have been concentrated on devices and circuits from that layers and their electrical characterization.

Nanosil - SWOT analysis



Strengths <ul style="list-style-type: none">-Advanced research/RI for long term Nanoelectronics at network level with critical interdependencies (=>Convergence MM/BC + MtM: Nanofunction, FET-F GA)-Strengthening of the European structuring	Weaknesses <p>Position of the European industry in the field of More Moore, however big companies are still very active: ST, Intel, Global Foundries, Micron...</p>
Opportunities <ul style="list-style-type: none">-Can, together with Sinano Institute, strengthen the European academic and scientific community compared to international competitors => ENI2-Can lever strong nationally funded and other European programmes-Can strengthen the cooperation with non-EU companies working in the EU	Threats <p>Difficulty to combine European and National funding, which depends on National policy, and to link FP, ENIAC and CATRENE Programmes:</p>