NANOSIL WP-4

JOINT CHARACTERIZATION AND MODELLING PLATFORM

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Outline

- **S.O.A.**
- Highlights 2010
- Recommendations from Reviewers
- Publications

State of the Art

- Full Quantum Models
  - Self consistent Quantum simulations based on the tight-binding Hamiltonian of NW [M. Luisier 2006]. Interface roughness in NWs [Poli 2008]. Non-parabolicity effects in NW [Gnani 2007]. **Full-quantum approach recently employed for the analysis of tunnel FETs [M.Luisier, 2009, M.Shin 2009].**
- Semi-classical models
  - MSMC for bulk, UTB SOI, FinFET, NW, n- and p-MOSFETs [De Michielis 2009]. kp-BTE solver for p-MOSFETs [Pham 2008]. These approaches can deal with arbitrary crystal orientations, strain, high-k dielectrics on mobility and high field transport [Ponton 2006, Serra 2009, Toniutti 2008]. Wigner Solvers include Source/Drain tunnelling and heterojunctions [D.Ferry 2000, Querlioz 2009]. Innovative Deterministic solution of the BTE in Si NWFETs [Jin 2008, Lenzi 2008, Gnani 2008]. **Studies on new channel materials for CMOS based on the Monte Carlo approach [Conzatti 2010] or on the deterministic solution of the 2D BTE [Pham 2007].**

State of the Art cont.

- Mobility models
  - Biaxially strained n-MOSFETs results still under debate: at large effective fields *ad hoc* reduction of the surface roughness spectrum. Smoother intergace experimentally reported using AFM measurements [Bonno 2008] and theoretically predicted using *ab-initio* calculations [Hadjisavvas 2007]. Controversial n and p results at low temperature in [Zhao 2009]: only electron mobility is enhanced. Recent results on the effects of biaxial strain on the Coulomb limited mobility [Weber 2008, Chen 2008, Driussi 2009]. **New measurements aimed at the morphological characterization of the strained Si to SiO_2 interface [Zhao VLSI 2009]. The mobility calculations obtained by using directly the measured roughness spectrum show a fairly good agreement with the experiments [Zhao TED 2010].**
  - Use of advanced simulation tools for the design and optimization of strain-induced mobility enhancements in FinFETs using MSMC [Serra 2009]
  - High-k related mobility degradation. Originally attributed to remote optical phonons [Fischetti 2001]. Recently more emphasis on Coulomb centers and interface defects produced by nitrogen diffusion [Fischetti

State of the Art (cont.)

- **Compact models**
  - Recent Compact Models for MG-MOSFETS [Iñiguez 2006, Ortiz-Conde 2007, Song 2009]. Short channel effect based on full 2D or 3D analysis [Børli 2009]. QME recently introduced for UTBSOI [Tang 2009]. AC models still based on the long-channel model [Lázaro 2009]. Compact Models for SB-MOSFETS (tunneling) just started [Balaguer 2010]. Very little work accomplished for strained MG-MOSFETs.
- **Experimental characterization**
  - Open problems in nano-MOSFETs with high-k and M-Gate: EOT evaluation (HF CV), small area interface characterization (LF noise measurements [Bennamane 09]), mobility measurement in short channel and leaky MOSFETs [Trojman 09], magneto-resistance mobility measurements [Casse 09], increasing role of parasitic source-drain or gate series/access resistances and new methodologies for Rsd extraction [Fleury 09].

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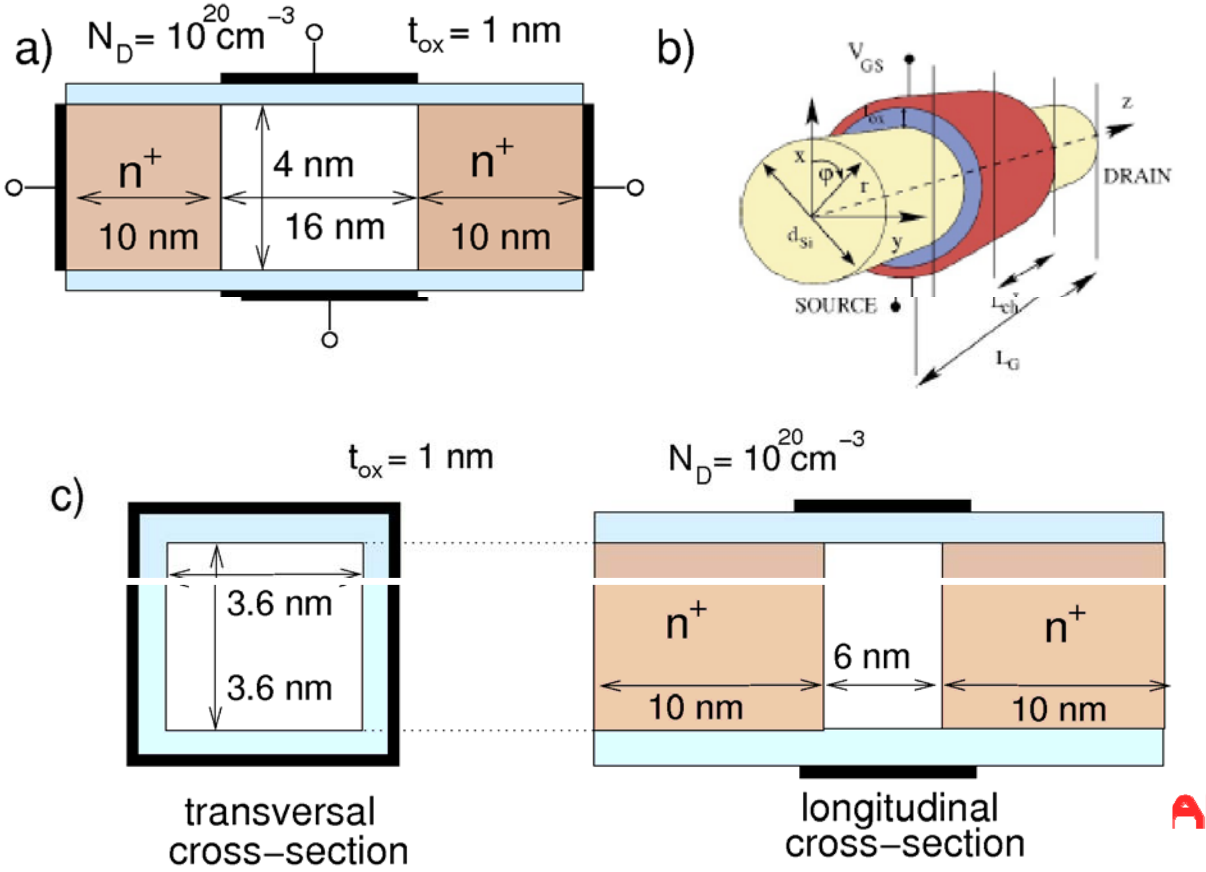
Highlights 2010

- A comprehensive set of tools, including full-quantum models, and template devices, representative of the 16nm node, have been tested and compared (D4.6).
- Compact model development taking into account: i) Electrostatics, ii) Partially ballistic transport and iii) Variability. The activity was carried out in close cooperation with the WP4 partners which provided TCAD simulations for the template devices (D4.5).
- Comparison of strained Ge MOSFETs w.r.t. to unstrained and strained silicon transistors has unrevealed the potentials of the former.
- A new technique was developed for the experimental extraction of the threshold voltage VT in nanoscale transistors. Robustness of the proposed method was demonstrated on experimental data from advanced FinFETs and UTB SOI MOSFETs.
- Modeling of devices with Shottky barrier S/D

TOOL BENCHMARKING
(a) Structure of the simulated DG-FET (Lg= 16 nm). (b) Cylindrical and (c) Rectangular gate all-around structures of the SNW-FET.



Transport models

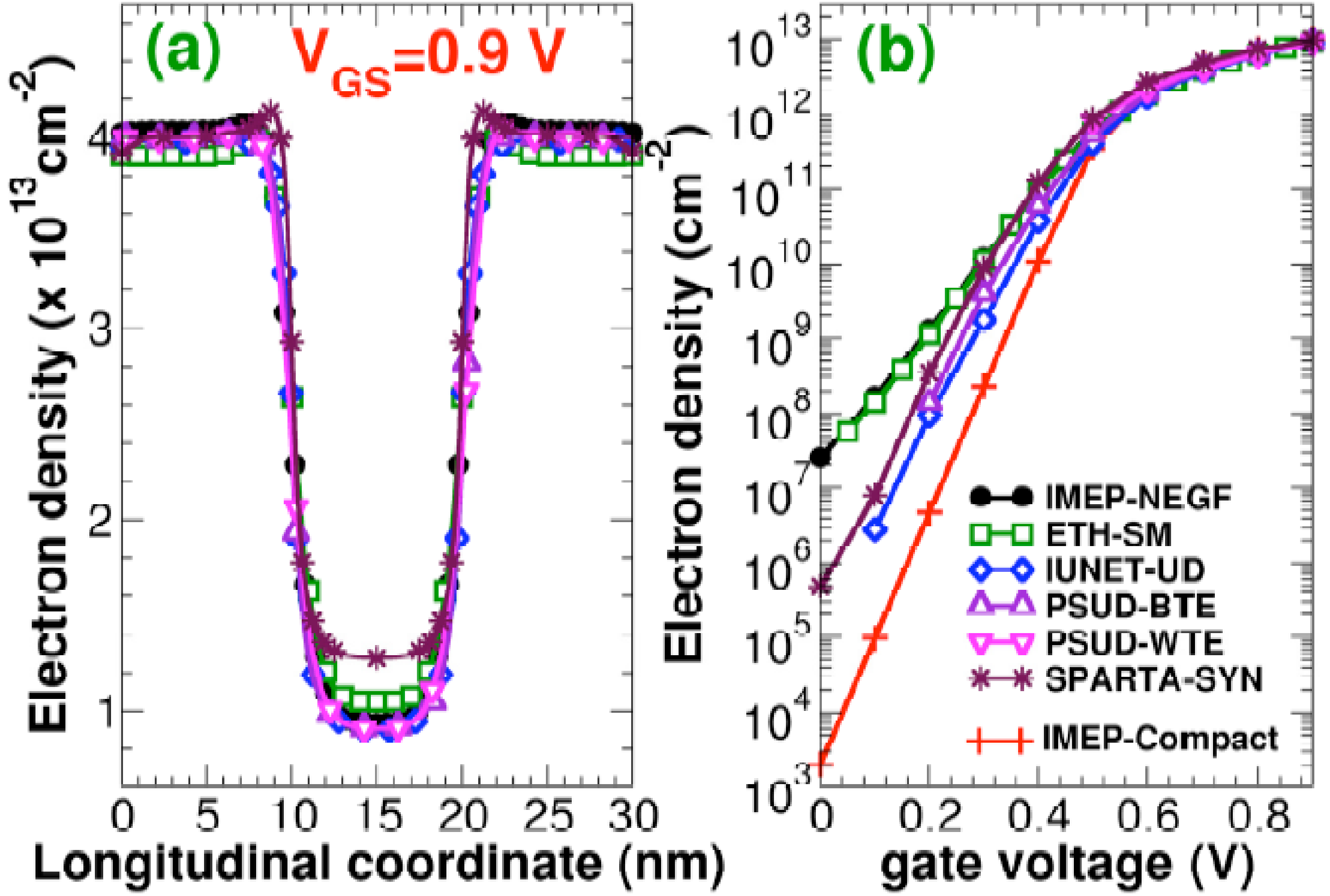
- Multi-Subband Monte Carlo (IUNET-UD)
- 2D-3D Non-equilibrium Green's Functions (IMEP-NEGF)
- Semiclassical Monte Carlo (SPARTA-SYN)
- Scattering Matrix with effective mass approximation (ETH-SM)
- Multi-subband MonteCarlo for BTE and Wigner transport equation (PSUD-BTE and PSUD-WTE)
- Analytical Natori-based model (IMEP-Compact)

Main findings: S/D tunneling

- Both for the 10 nm double-gate MOSFET and for the 6 nm nanowire FET, source-to-drain tunneling is extremely important, especially in evaluating the subthreshold behavior.
- Not considering tunneling and wave function penetration in the gap can result in the inability to recover the actual subthreshold behavior.

Electrostatic and S/D tunneling

V_{DS}=0 V, L_g=10 nm



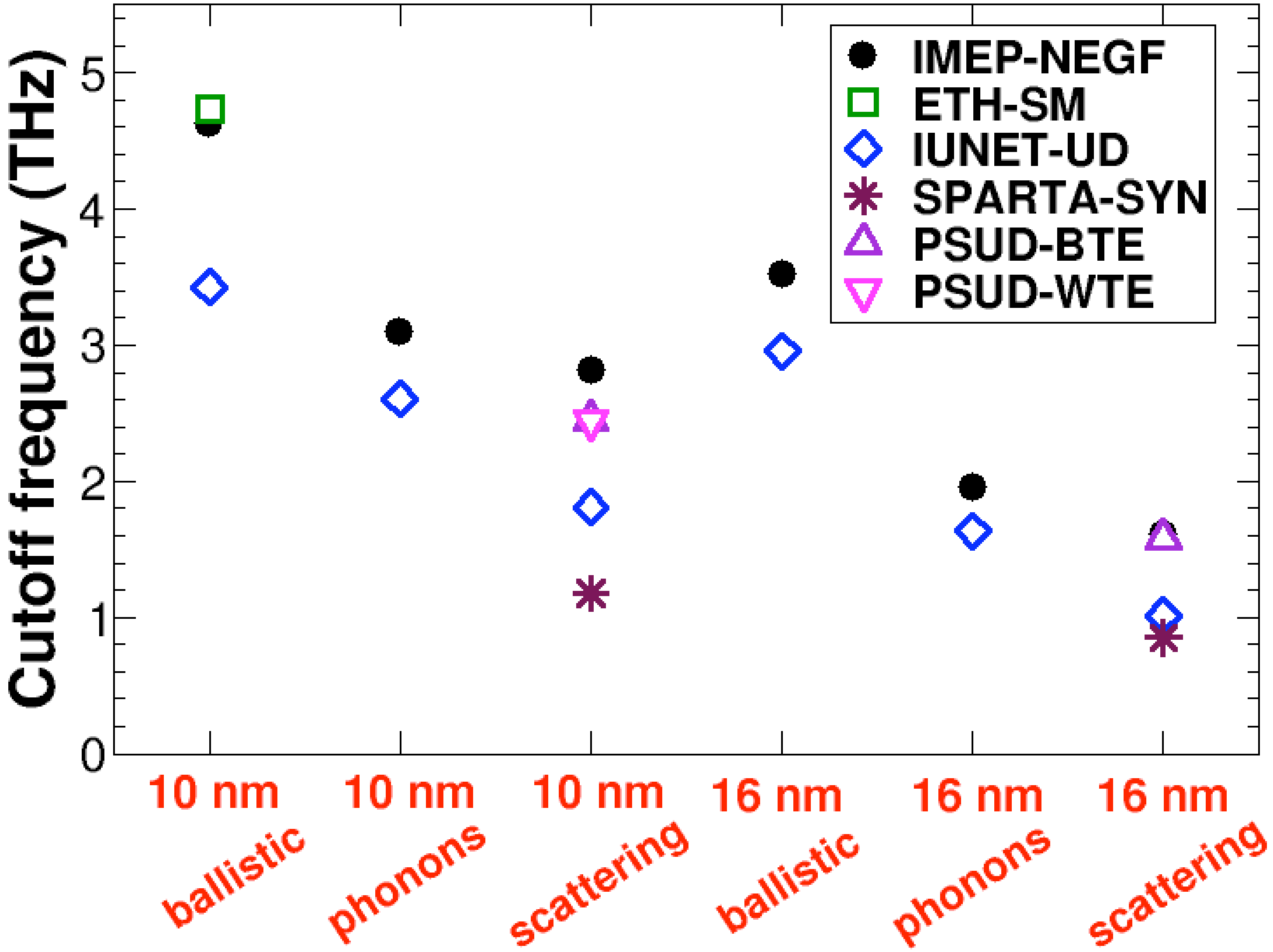
Semi-ballistic transport

All considered devices far from fully ballistic transport.

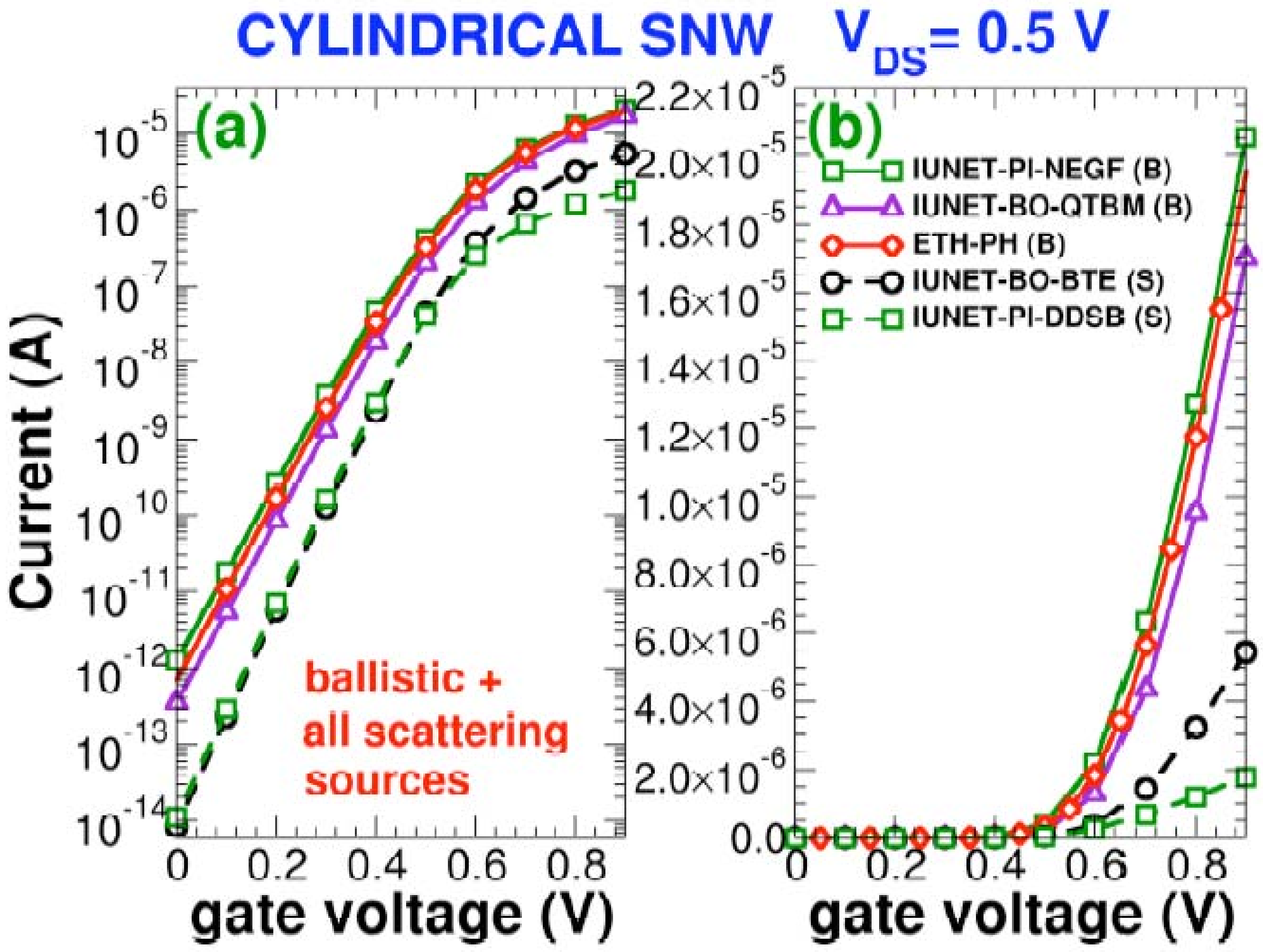
The cutoff frequency of the intrinsic device (i.e., excluding parasitic capacitances) is cut by roughly a factor two when the main scattering mechanisms are considered, but still above the THz range

Cutoff frequency

DG MOSFET V_{DS}=0.5 V



Current drive



Silicon-based nanostructures and nanodevices

Scattering mechanisms and transport models

Assumptions on the scattering mechanisms are apparently at least as important as the adopted transport model.

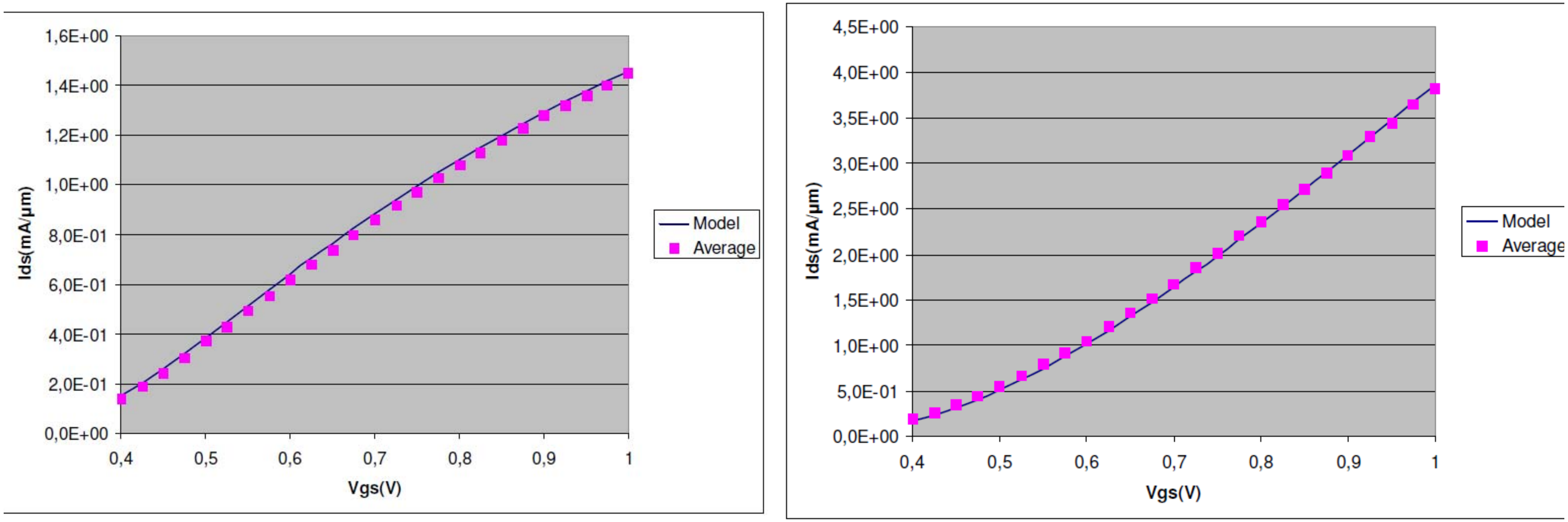
Indeed, differences among results obtained with different transport models are limited from a qualitative point of view: by performing different calibrations, all transport models considered should be able provide the same current-voltage characteristics.

	3D-Monte Carlo (SPARTA-SYN)	Multi-Subband Monte Carlo (IUNET-UD, PSUD-BTE)	Deterministic 1D BTE (IUNET-BO-BTE)	Ballistic full quantum transport model (ETH-SM, IUNET-PI-NEGF, UGLA, IUNET-BO-QTBM)	NEGF non-ballistic (IMEP-NEGF, ETH-PH)	Drift-Diffusion transport per 1D subbands (IUNET-PI-DDSB)	Wigner-Transport equation (PSUD-WTE)
Double Gate FET	Electrons treated as free carrier gas; Full-band structure considered. Appropriate for high field analysis, provides adequate corrections for quantum effects. Numerically efficient: allows for time dependent and RF analysis [TED2007_2] Orientation and strain effect only included empirically	Accounts for quantization in the vertical direction (subband splitting and carrier gas degeneracy, subband repopulation, effect on scattering rates). Theoretical framework naturally extended to SOI single and double gate devices. Physical models for technology boosters such as strain, alternative channel and gate-stack materials are already available. Computational complexity is weakly dependent on the channel length. Quite inefficient in the simulation of the sub-threshold region. Difficult to include band to band tunnelling that may influence the off-current of the transistor.	Not applicable	The Schrödinger (envelope) equation in the effective mass approximation and the Poisson equation are solved iteratively up to self-consistency between charge density and electrostatic potential. The inclusion of open boundary conditions for the charge transport is accomplished by the Scattering Matrix Approach (SMA) [Heinz_JAP] or by means of the NEGF formalism. Only elastic scattering are taken into account, while inelastic scattering are neglected. Both inter and intra subband scattering are considered. IUNET-BO-QTBM is not applicable	As the model in the previous column, but additional scattering mechanisms are taken into account: electron-phonon, surface roughness and ionized impurities.	Not applicable	As the Multisubband Monte Carlo model, but the Wigner-Boltzmann transport equation is solved instead of the BTE. The non-parabolicity effect is not included as well as the penetration of the wave function into the oxide. Quantum effects are considered in some extents. Computationally demanding.

short channel SNW-FET	As above	For a Multi-subband Monte Carlo approach the long or short devices can be simulated with no major differences. For uniform transport simulations periodic boundary conditions in the transport direction can be used so that a 2D rather than a 3D Poisson solver can be used.	Very useful when one wants to obtain mobility and Ion in cylindrical nanowires by accounting for a realistic description of the scattering rates [TED2008-1, JCE2008]. In addition, a rigorous analytical solution of the 1D BTE for SNWs under quasi-ballistic condition has been recently worked out: a very fast methodology to obtain rigorous functional dependencies of the expected effective mobility and backscattering coefficient [TED2008-2, SISPAD2008, SISPAD2009, ESSDERC2009, PICE-SYMP-2009, TED2010]	As above. For what concerns the IUNET-BO-QTBM, the 1-D open-boundary Schrödinger equation is solved for each subband of the cylindrical SNWT. No surface roughness considered. Band non-parabolicity is taken into account. [Gnani2007].	As above: in this case 2D Schroedinger equation is solved in the transversal direction, and transport is computed along 1D subbands.	The transport equation and the continuity equation in the DD approximation in stationary conditions and neglecting generation recombination processes are solved self-consistently. Fast as compared to Monte Carlo models. Not accurate for high longitudinal electric fields.	Not applicable

Compact Models D4.5

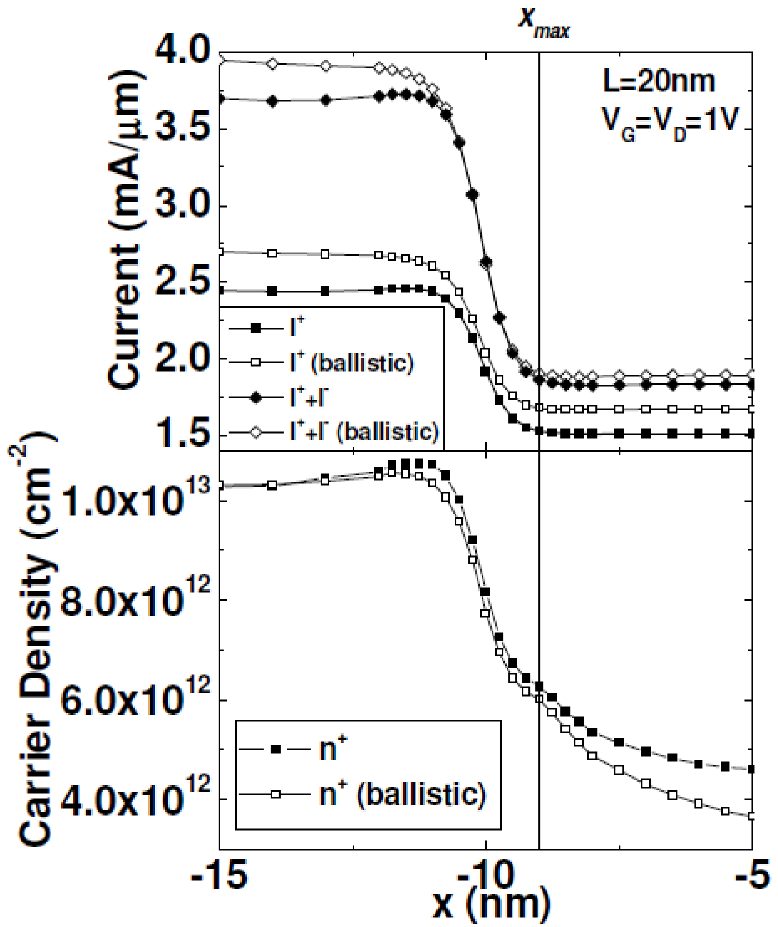
- Three main issues: i) Electrostatics, ii) Partially ballistic transport and iii) Variability.
- Multi-gate devices: double-gate, tri-gate, gate-all-around, ultra-thin body.
- All models are favourably compared with a series of TCAD simulations and experiments.



(a)

(b)

Comparison of modelled characteristics and simulated data using average simulated values from NANOSIL WP4 teams for VDS=0.1V (a), and VDS=1V (b), and the template n-channel 16 nm DGMOSFET



Directed currents (top) and carrier density (bottom) along the device in the ballistic and not ballistic case. It is evident that assumption of Eq. 8 (proposed model) is better verified than assumption of Eq. 5 (LM) (1.2% versus 9.3%). Moreover, the assumption of Eq. 6 (or 9) (LM and proposed model) is well verified (4.3%)

Alalytical models for variability

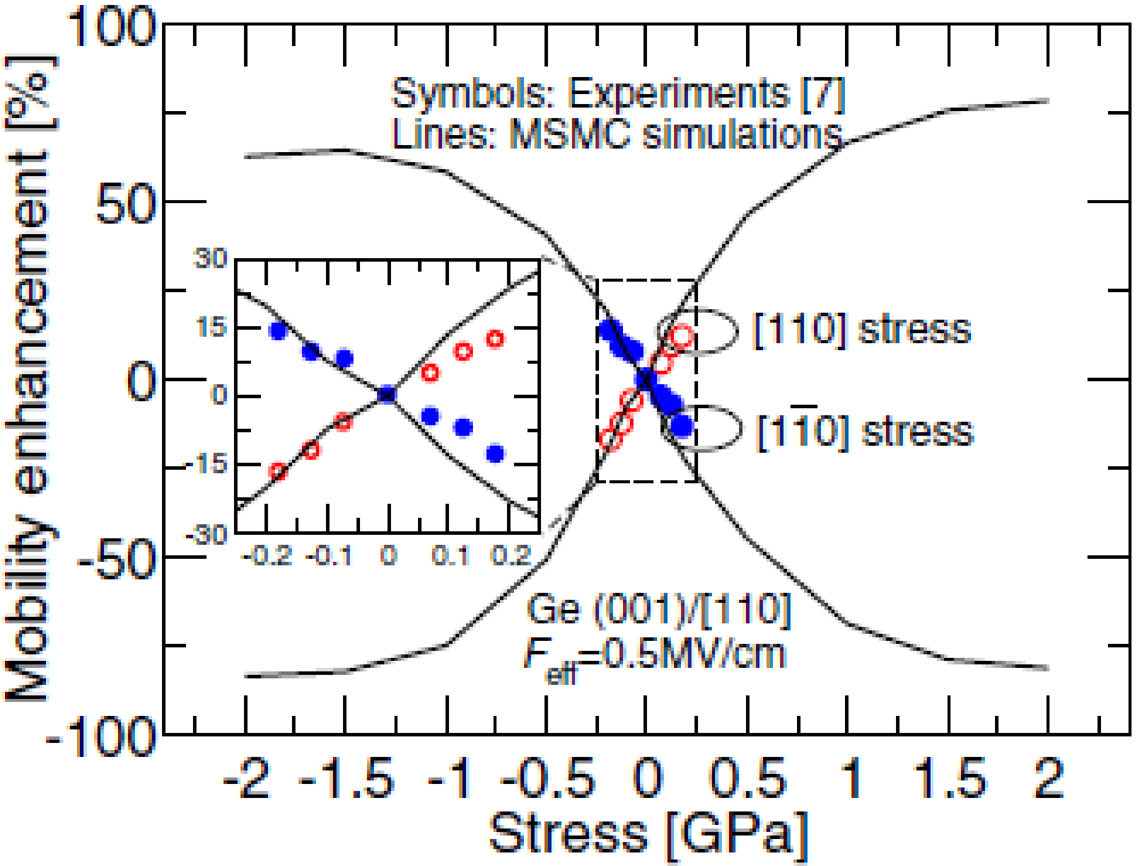
	Vds = 50 mV	**Approach**		
		An.An	***An.TCAD***	***Atom[Cheng 2008]***
32 nm	σ_{Vth} LER (mV)	2.96	3	3.3
	σ_{Vth} SR (mV)	0.23	0.25	N/A
22 nm	σ_{Vth} LER (mV)	6	5.6	5.8
	σ_{Vth} SR (mV)	1.4	1.4	N/A

	Vds = 1V	***Approach***		
		An.An	***An.TCAD***	***Atom[Cheng 2008]***
32 nm	σ_{Vth}LER (mV)	7.9	8.3	8.6
	σ_{Vth}SR (mV)	0.66	0.6	N/A
22 nm	σ_{Vth}LER (mV)	14	13.6	13
	σ_{Vth} SR (mV)	4.3	4.4	N/A

I_{ON} of Ge MOSFETs compared to Si MOSFETs

- Comprehensive semi-classical transport model for nMOS and pMOS including:
  - Phonons, Surface Roughness
  - High-k related scattering mechanisms
  - Non-conventional crystal orientations
  - Strain effects through band-structure modifications
  - Realistic series resistances
- Validation of models against exp. data
- Comparison of Ion in Ge and sGe versus Si and sSi nano-scale n- and p-MOSFETs

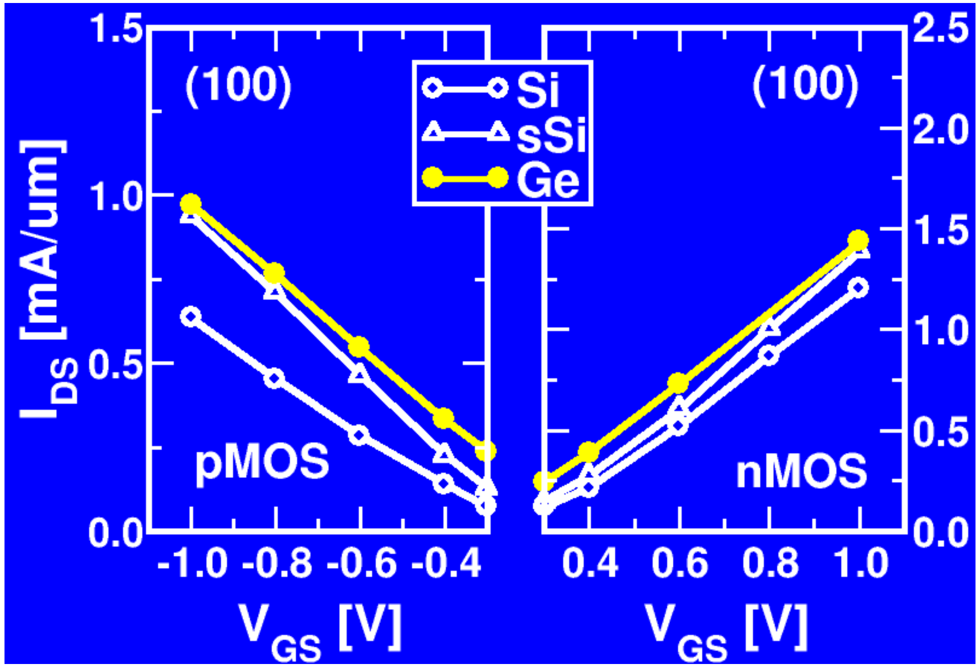
The simulation results have shown that strained Ge *n*-MOSFETs have great potentials for beating the Si counterparts, however the engineering of the series resistance is a crucial issue.

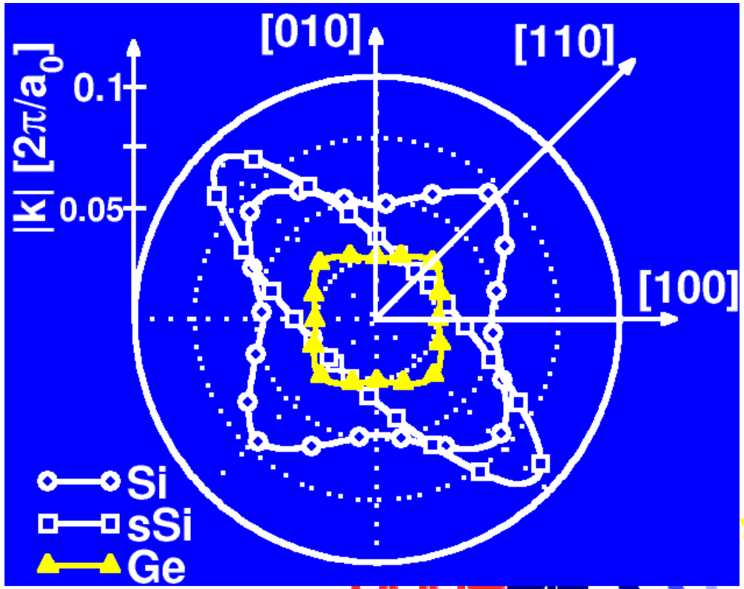


(100)/[110] Ge. Measured (symbols, [M. Kobayashi *et al. IEEE TED*, p. 1037, 2010]) and simulated(lines) electron mobility vs. uniaxial tensile stress along the [110] and [110] directions and at *F*eff=0.5MV/cm. The inset shows a zoom for low stress values. The simulated mobility enhancement saturates at about 1.5GPa.

On Current in Si, sSi and Ge devices

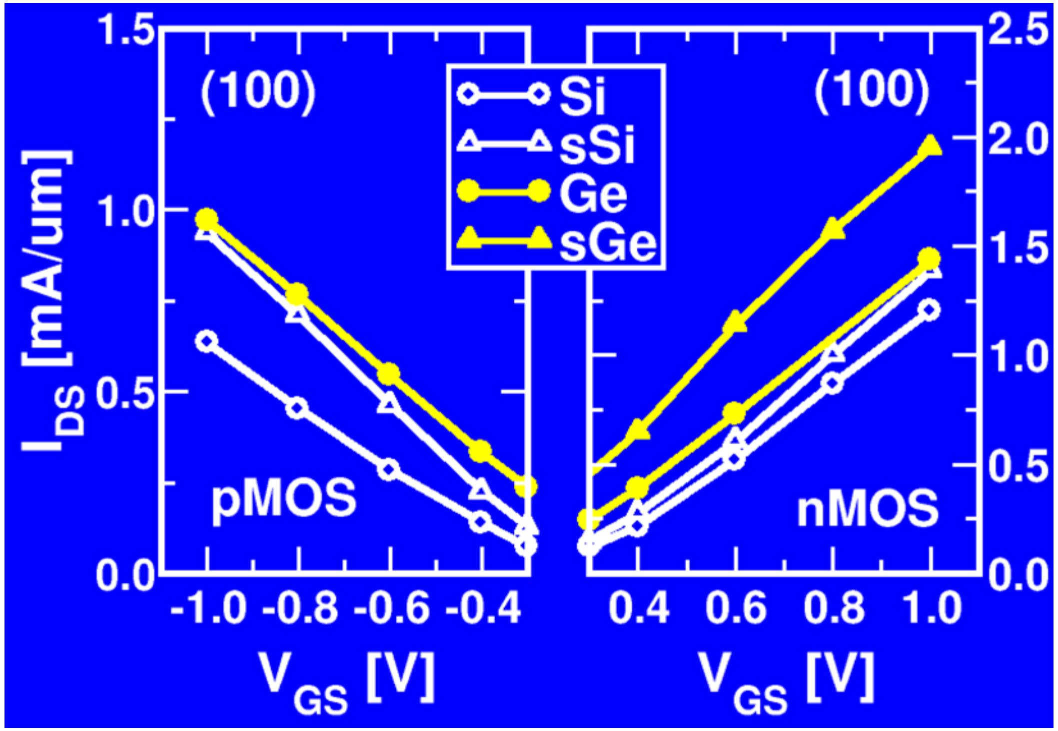
- **(100)/[110] oriented DG-MOSFETs**
- **1.5GPa tensile/compressive stress along the transport direction for n/p devices**
- **Comparable hole effective mass along [110] direction for both** sSi **and Ge**



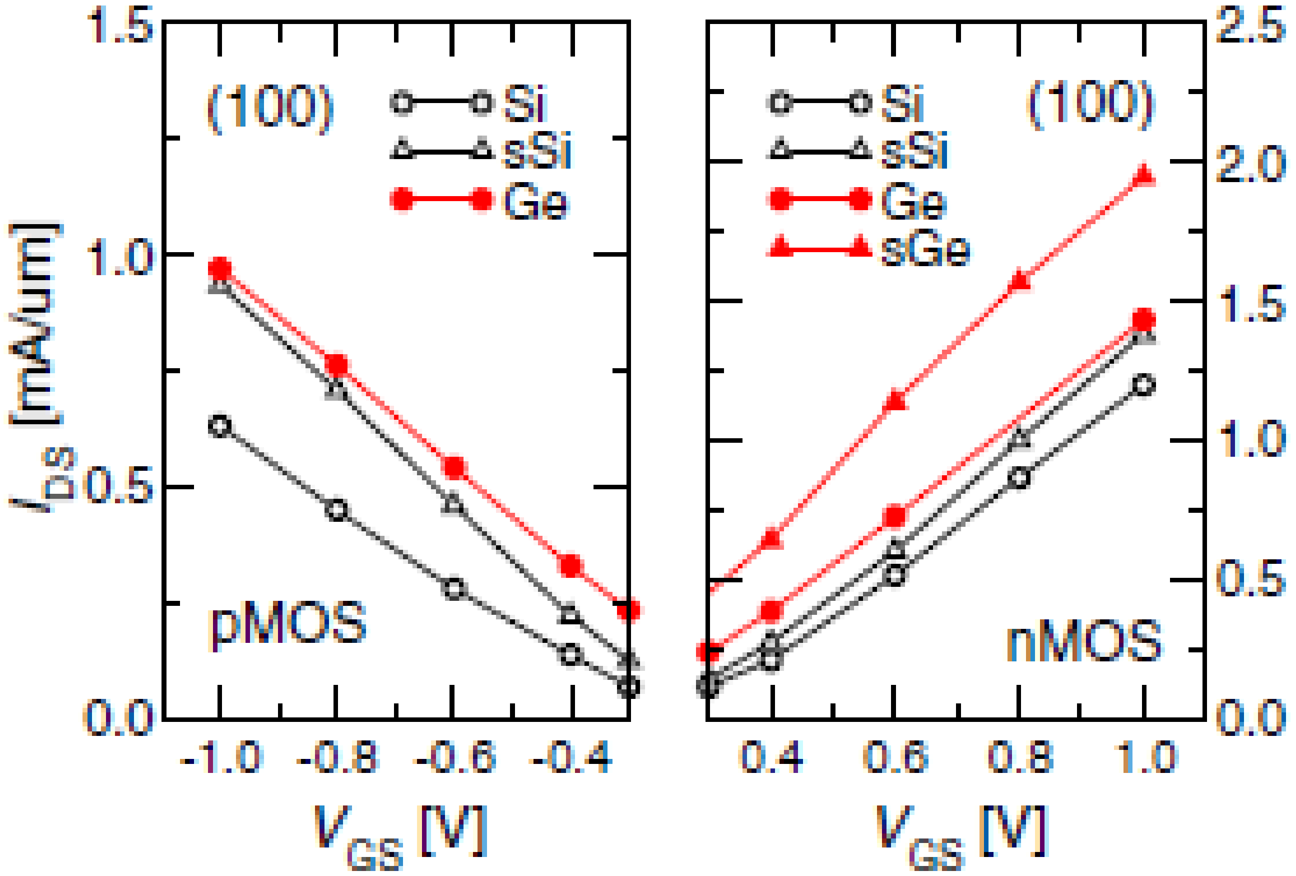


Ion in Si, sSi, Ge and sGe devices

- **(100)/[110] oriented DG-MOSFETs**
- **Comparable hole effective mass along [110] direction for both sSi and Ge**



NANOSIL Silicon-based nanostructures and nanodevices



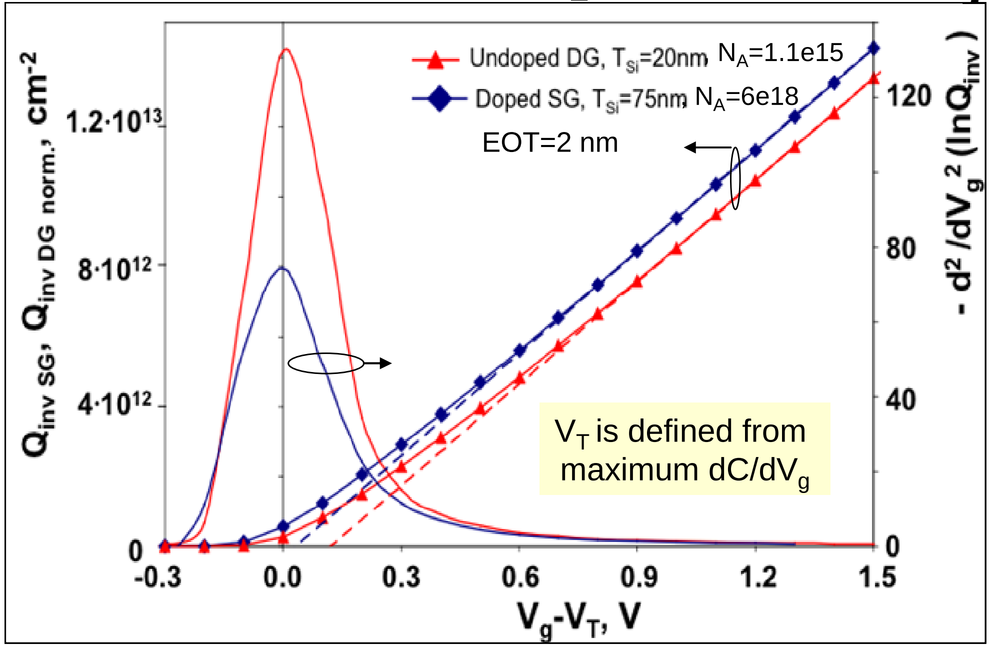
Simulated drain current versus gate voltage for the 25nm DG device and for unstrained and strained Si and Ge (EOT=1nm, *TSI*=11nm).

Left: *p*-MOS. Right: *n*-MOS. The 1.5GPa stress is along the [110] transport direction and it is tensile and compressive for *n*-MOS and *p*-MOS, respectively.

Example of new characterization technique

- A new technique was developed for the experimental extraction of the threshold voltage V_T in nanoscale transistors. Robustness of the proposed method was demonstrated on experimental data from advanced FinFETs and UTB SOI MOSFETs.

New technique – V_T extraction



V_T is defined from maximum dC/dV_g

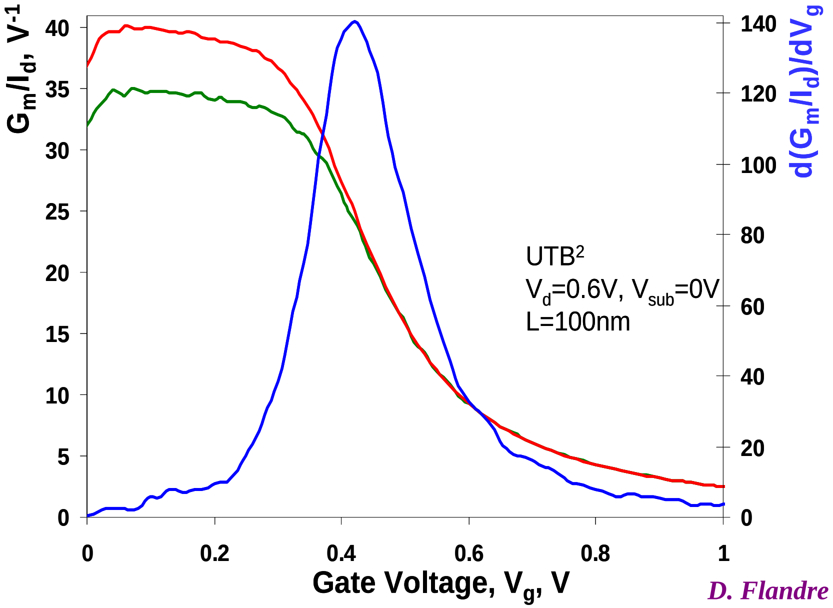
Based on the derivative of G_m/I_d

$$\boxed{\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right)=\frac{q}{kT}\frac{d^2\varphi_s}{dV_g{}^2}}$$

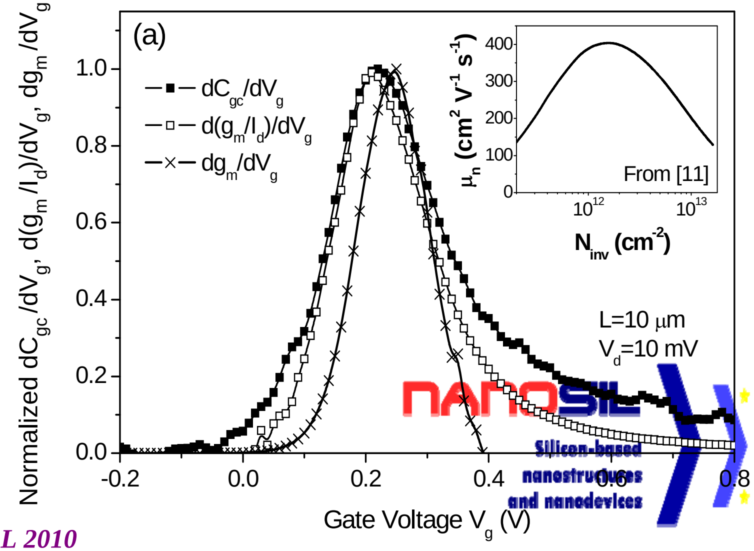
✓ ***as accurate as capacitance method***

✓ ***less sensitive to μ (V_g) and R_s effects***

✓ ***more adequate than linear extrapolation-based methods,*** *which give particularly large errors in the case of gradual transition between weak and strong inversion (i.e. thin oxides, undoped bodies)*



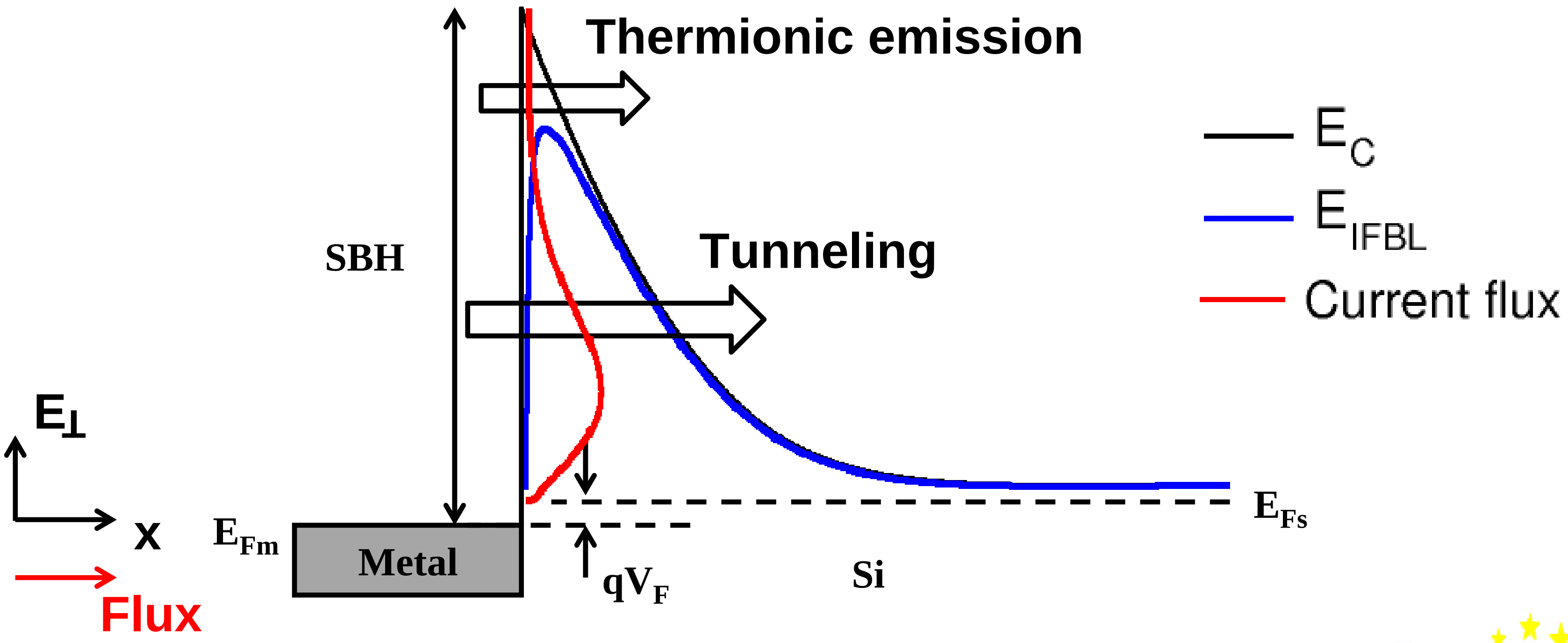
D. Flandre et al. IEEE EDL 2010



MS-Monte Carlo simulation of FDSOI Schottky barrier MOSFETs

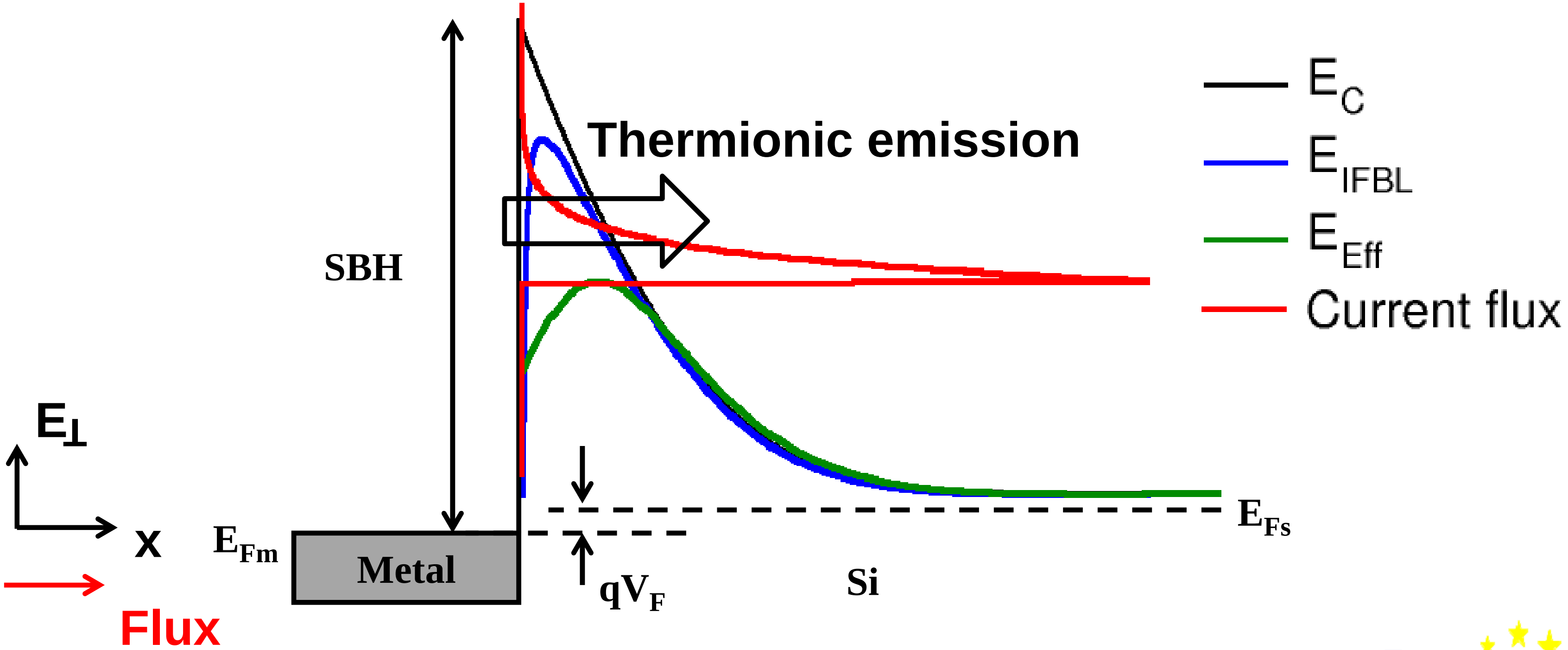
- Goal
  - Performance of short L_G SB-MOSFETs
- Approach
  - Multi Subband Monte Carlo
  - Implemented SB contacts in MSMC

Current transport across SB



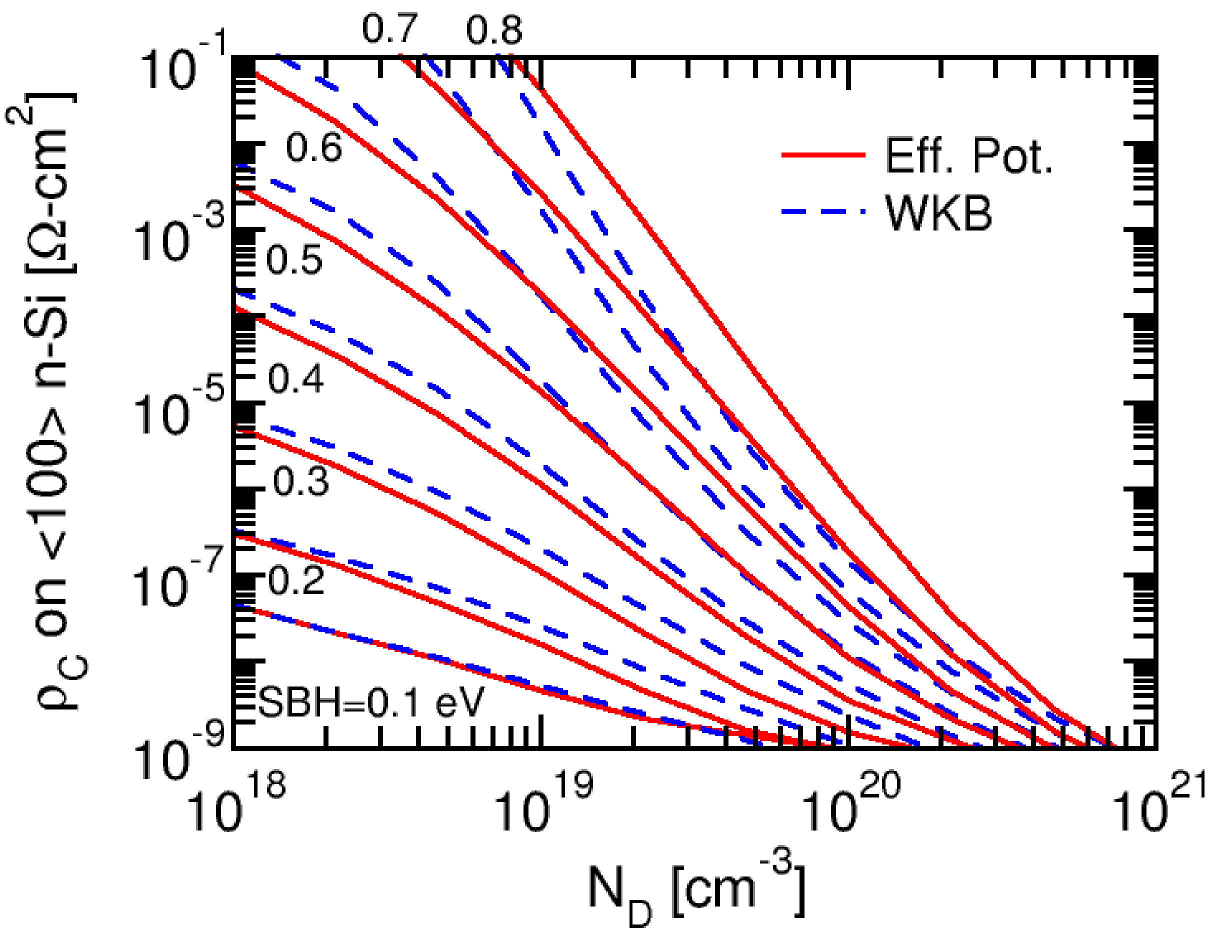
Effective potential method

$$E_{Eff}(x) = \int E_{IFBL}(x') \frac{1}{\sqrt{2\pi}a_0} \exp\left(-\frac{(x'-x)^2}{2a_0^2}\right) dx' \qquad a_0^2 = \eta^2/(8m^* k_B T)$$



- Need to compare to other tunneling model

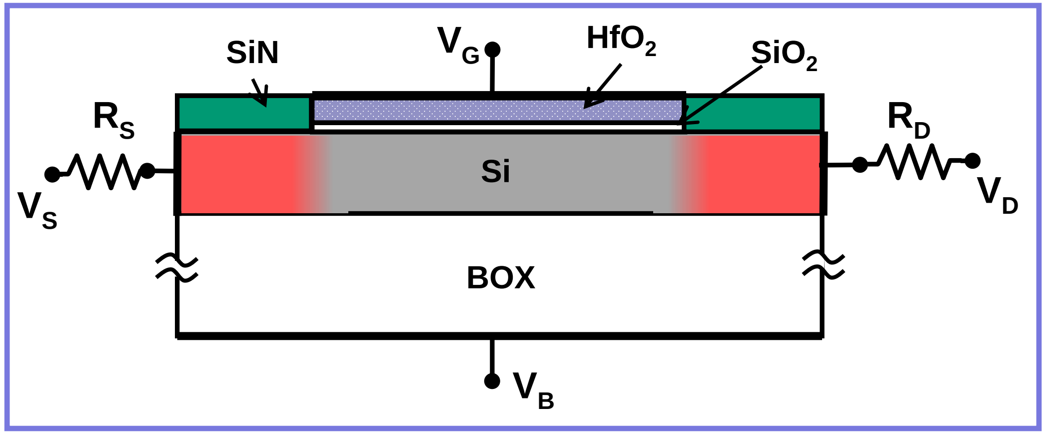
Eff. Pot. compared to WKB



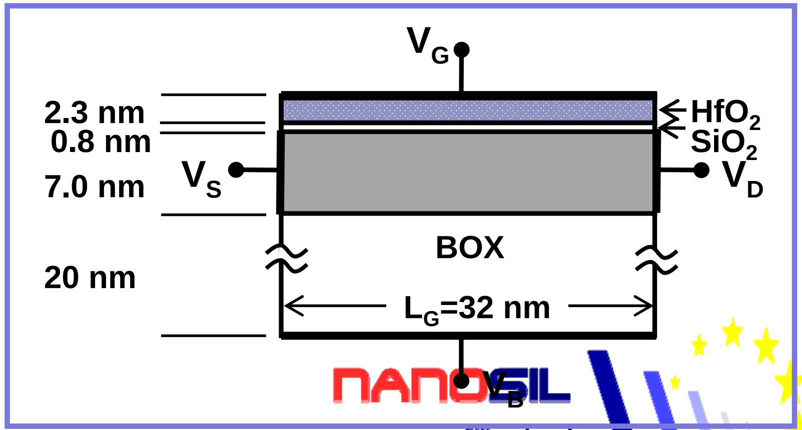
MSMC device design

- L_G=32 nm
- T_{Si}=7 nm
- EOT=1.2 nm
- Surface roughness + Phonon scattering
- Surface/channel orientation (001)/[100]

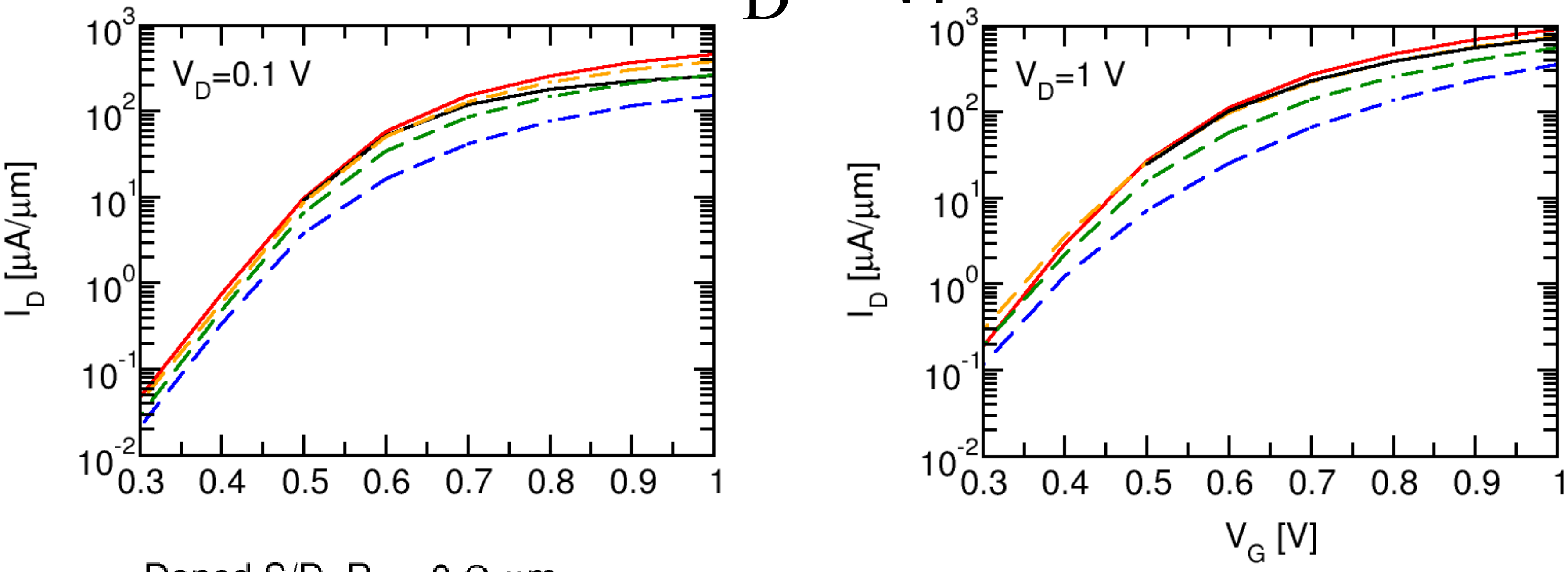
Doped Source/Drain



Schottky barrier Source/Drain

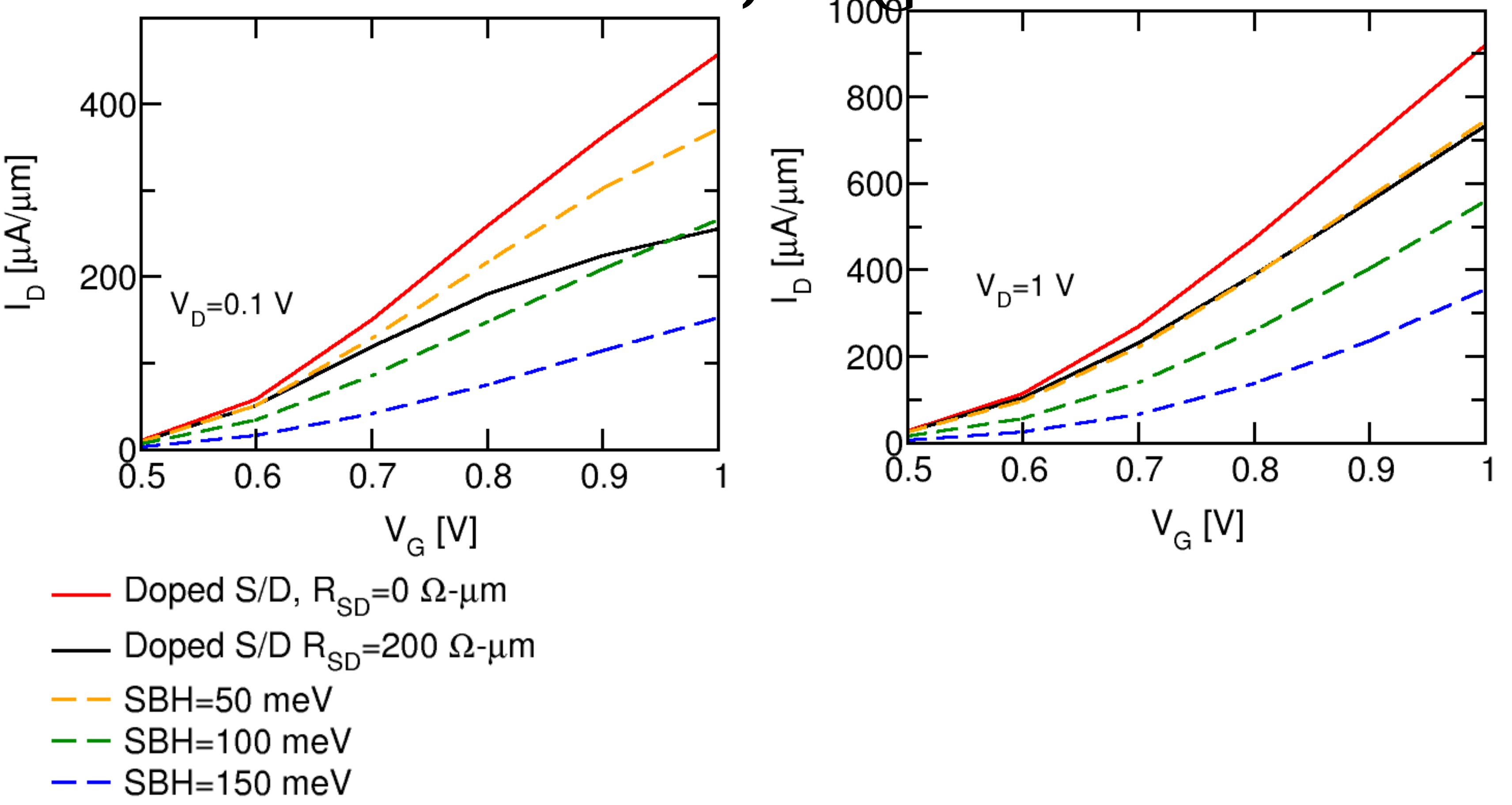


I_D-V_G

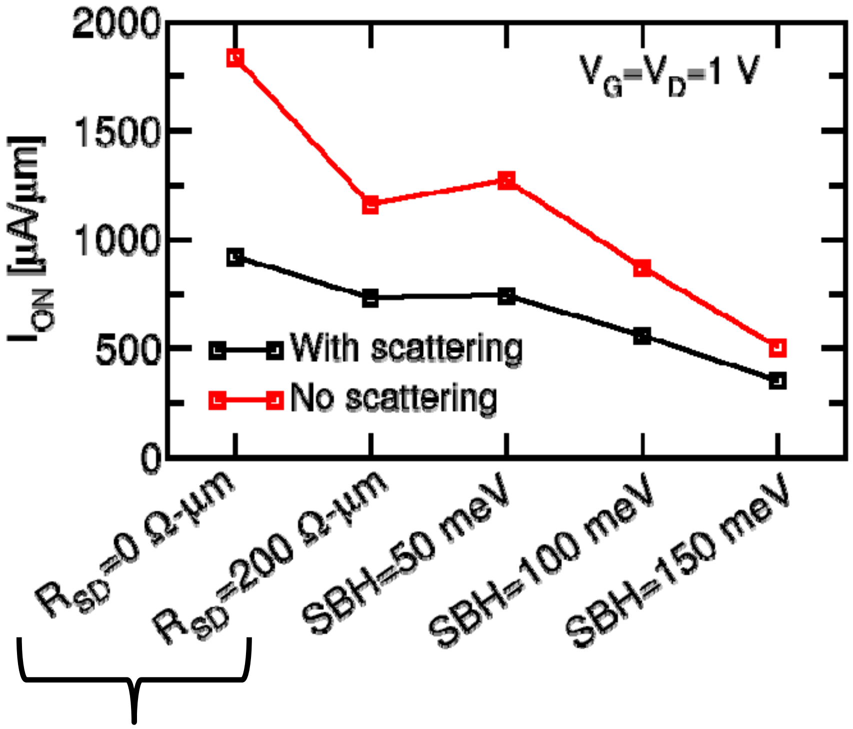


	SS @V_D=0.1 V (mV/dec)	SS @ V_D=1 V (mV/dec)	DIBL @I=0.3µA (mV/V)
Doped	82	85	56
SBH=50 meV	82	93	80
SBH=100 meV	82	94	71
SBH=150 meV	82	97	61

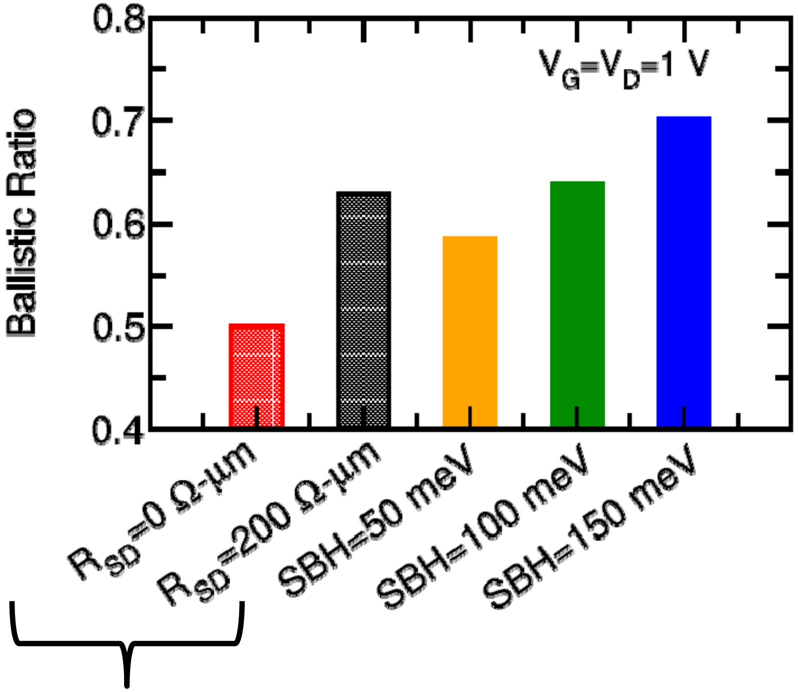
I_D-V_G


I_D [µA/µm]
400
200
0
0.5
0.6
0.7
0.8
0.9
1
V_G [V]
V_D=0.1 V
1000
800
600
400
200
0
0.5
0.6
0.7
0.8
0.9
1
I_D [µA/µm]
V_G [V]
V_D=1 V
Doped S/D, R_{SD}=0 Ω-µm
Doped S/D R_{SD}=200 Ω-µm
SBH=50 meV
SBH=100 meV
SBH=150 meV

Compare to ballistic simulation



Doped S/D



Doped S/D

NANOSIL
Silicon-based nanostructures and nanodevices

Conclusions

- Effective potential method to treat SB tunneling presented
  - In good agreement with WKB
  - Implemented in MSMC
- SBH <50 meV needed to outperform R_{SD}=200 Ω-µm
- Increasing SBH
  - SB-MOSFETs closer to ballistic limit
  - ON current limited by injection

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Response to the recommendations of the second Review Report

- ***Recommendation 4***

- *In WP4 the partners should use appropriate figures of merit for device operation, and not concentrate overly on carrier mobility as a means of comparison of likely performance.*

- In order to address the Reviewers recommendation according to which the partners of WP4 should use appropriate figures of merit for device operation, the deliverable D4.6 on the bechmarking between full quantum and semi-classical transport models was focused primarily on the comparison of complete I_{DS} versus V_{GS} and V_{DS} curves and also on the cutoff frequency that are very relevant for RF applications.

2010 WP4 Publications

- 19 IEEE TED or EDL Journal publications
- 4 IEDM publications
- 63 (23 joint) Journal publications