

ANNEX 2 References

A2.1. Books/Book chapters (joint): 2+12

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date
1	Book	INPG/FMNT (Editor), Almost all partners (see D5.4 for details)	ISTE-Wiley book (650 pages)	Nanoscale CMOS: Innovative Materials, Modeling and Characterization	1-4	2010
2	Book	Tyndall, ISP-Kiev, INPG/FMNT, UCL, UGR	Springer (450 pages) Doi : 10.1007/978-3-642-151868-1	Semiconductor-On-Insulator Materials for NanoElectronics Applications	1, 2, 4	2011
3	Book chapter	O. Engstrom Chalmers, LIVUNI, Tyndall, AMO	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 2 : Gate Stacks	1,3	2010
4	Book chapter	B. Majkusiak et al WUT, IUNET, ETZH	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 7: Modeling and simulation approaches for gate current computation	4	2010
5	Book chapter	Q. Raffhay et al. INPG, IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 9: Modeling of end of the roadmap nMOSFET with Alternative channel material	4	2010
6	Book chapter	Martinez et al INPG, GU	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 10: NEGF for 3D device simulation of nanometric inhomogenities	4	2010
7	Book chapter	G. Iannaccone et al, IUNET, INPG	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 12 : Beyond CMOS	4	2010
8	Book chapter	P. Hurley et al Tyndall-UCC, Chalmers, INPG	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 15: Characterization of interface defects	4	2010
9	Book chapter	Lecestre et al. IEMN/ISEN, STM	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Confined and guided vapor-liquid-solid catalytic growth of Silicon nanoribbons: from nanowires to structured silicon-on-insulator layers	2	2011
10	Book chapter	Afzalian, et al. UCL, Tyndall-UCC	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Gate modulated resonant tunneling transistor (RT-FET): performance investigation of a steep slope, high on-current device through 3D non- equilibrium green function simulations", chapter in "Semiconductor-On-Insulator Materials for NanoElectronics Applications"	4	2011
11	Book chapter	T. Rudenko et al ISP-Kiev, UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Special features of the back-gate effects in ultra-thin body SOI MOSFETs", chapter in "Semiconductor-On-Insulator Materials for NanoElectronics Applications"	4	2011
12	Book chapter	M. Bawedin et al. INPG, Leti	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Floating-body SOI memory: the scaling tournament"	4	2011
13	Book chapter	S. Cristoloveanu et al. INPG, Leti, ST	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "A selection of SOI puzzles and tentative answers"	4	2011
14	Book chapter	W. van den Daele et al INPG, IMEC	Wiley (S. Luryi et al. eds) "Future Trends in Microelectronics, from Nanophotonics to Sensors and Energy"	GeOI as a platform for ultimate devices	1, 4	2010

A2.2. Book chapters (single-partner): 21

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date
1	Book Chapter	D. Leadley et al Warwick	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 1: Introduction to Part 1: Novel materials for nanoscale CMOS	1	2010
2	Book chapter	D.R. Leadley, et al Warwick	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 3: Strained Si and Ge Channels	1	2010

3	Book chapter	S. Mantl, D ; Buca, FZJ	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 4: From thin Si/SiGe buffers to SSOI	1	2010
4	Book chapter	E. Dubois et al, IEMN/ISEN	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 5: Introduction to Schottky-barrier MOS architectures: concept, challenges, material engineering and device integration	1	2010
5	Book chapter	E. Sangiorgi IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 6: Introduction to Part 2: Advanced modeling and simulation for nano-MOSFETs and beyond-CMOS devices	4	2010
6	Book chapter	M. Vasicek et al. IUNET	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 8: Modeling and simulation approaches for drain current computation	4	2010
7	Book chapter	B. Iniguez et al. URV	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 11: Compact models for advanced CMOS devices	4	2010
8	Book chapter	D. Flandre UCL	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 13: Introduction to Part 3: Nanocharacterization methods	4	2010
9	Book chapter	M. Mouis INPG	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 14: Accurate determination of transport parameters in sub-65 nm MOS transistors	4	2010
10	Book chapter	A. O'Neill et al. UNEW	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 16 : Strain determination	4	2010
11	Book chapter	D. Flandre et al. UCL	Book, "Nanoscale CMOS: Innovative Materials, Modeling and Characterization", ISTE – Wiley	Chapter 17: Wide frequency band characterization	4	2010
12	Book chapter	J.-P. Raskin UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "SOI SMOS: A mature and still improving technology for RF applications"	4	2011
13	Book chapter	F. Balestra INPG	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Silicon-based devices and materials for nanoscale FETs"	1-4	2011
14	Book chapter	F. Gamiz et al. UGR	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on « Ultrathin n-channel and p-channel SOI MOSFETs"	4	2011
15	Book chapter	J.-P. Colinge et al. Tyndall-UCC	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Junctionless transistors: physics and properties"	2, 4	2011
16	Book chapter	H.-N. Nguyen et al UPS	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Ohmic and Schottky contact SNTFET: transport properties and device performance using semi-classical and quantum particle simulation"	2, 4	2011
17	Book chapter	M. Pala, INPG	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on « Quantum simulation of Silicon-Nanowire FETs"	2, 4	2011
18	Book chapter	G. Gibaudo, INPG	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on "Mobility characterization in advanced FD-SOI CMOS devices"	4	2011
19	Book chapter	J.-P. Raskin et al UCL	Semiconductor-On-Insulator Materials for NanoElectronics Applications, Springer	Chapter on " Sensing and MEMS devices in thin-film SOI MOS technology"	2	2011
20	Book chapter	INPG/FMNT	Wiley (S. Luryi et al. eds) "Future Trends in Microelectronics, from Nanophotonics to Sensors and Energy"	Silicon-based devices and materials for nanoscale CMOS and beyond-CMO, chapter in	1, 2, 4	2010
21	Publication	E. Kasper, USTUTT	Horizons in World Physics. Volume 273 (ISBN: 978-1-61728-995-8)	Positioning Ge-Dots on Si for Device Applications/Book chapter /pp. 171-185	2.4	2010

A2.3. Journal publications (joint): 32+8

NO.	Title	Main author, Partners involved	WP/ FP	Title of the periodical	Vol., No .	Year	Pages	Permanent identifiers DOI
1	Defect-related excess low-frequency noise in Ge-on-Si pMOSFETs	E. Simoen, et al Warwick, IMEC	1	Electron Device Letter	Vol 32	2011	pp 87-89	http://dx.doi.org/10.1109/LED.2010.2089968
2	A quasi-analytical model for anowires FETs with arbitrary polygonal cross section	L. De Michielis, et al IUNET, EPFL	4	Solid-State Electronics	Sept	2010	929 – 934	doi :10.1016/j.sse.2010.04.039
3	Physics of Gate Modulated Resonant Tunneling (RT)-FETs: Multi-Barrier MOSFET for Steep Slope and High On-Current	Afzalian et al UCL, Tyndall	4	Solid State Electronics		2011	pp. 50-61	doi :10.1016/j.sse.2011.01.016
4	Quantum Confinement Effects in Capacitance Behavior of Multigate Silicon Nanowire MOSFETs	A. Afzalian et al. : Tyndall, UCL	4	IEEE Trans. On Nano-technology	vol. 10, march	2010	pp. 300-309	10.1109/TNANO.2009.2039800
5	Low temperature tunneling current enhancement in silicide/Si Schottky contacts with nanoscale barrier width	N. Reckinger et al UCL, IEMN	1.2	Appl. Phys. Lett.	No 98, 2011	2011	112102	10.1063/1.3567546
6	Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs	V. Kilchytyska, UCL, IMEC	4	Solid State Electronics	Vol. 59, 2011	2011	pp. 18-24	10.1016/j.sse.2011.01.008

7	Experimental study of transconductance and mobility behaviors in ultra-thin SOI MOSFETs with standard and thin buried oxides	T. Rudenko, ISP_kiev, UCL, Leti	4	Solid State Electronics	Vol. 54, Feb. 2010	2010	pp. 164-170	10.1016/j.sse.2009.12.014
8	Substrate impact on threshold voltage and subthreshold slope of sub-32 nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel	S. Burignant, et al UCL, Leti	4	Solid State Electronics	Vol. 54, Feb 2010	2010	pp. 213-219.	10.1016/j.sse.2009.12.021
9	Gm/Id Method for Threshold Voltage Extraction Applicable in Advanced MOSFETs With Nonlinear Behavior Above Threshold	D. Flandre, et al UCL, ISP-Kiev	4	IEEE Electron Dev. Lett.	Vol. 31, Sept. 2010	2010	pp. 930-932	10.1109/LED.2010.2055829
10	Radio-Frequency Study of Dopant-Segregated n-Type SB-MOSFETs on Thin-Body SOI	C. Urban et al FZJ, UCL	1.1 & 1.2	Electron Device Letters	Vol. 32, Issue 6	April 2010	537 – 539	10.1109/LED.2010.2045220
11	Strain tensors in layer systems by precision ion channeling measurements	Trinkaus et al FZJ, Leti	1.1	J. of Applied Physics	Vol. 107 Issue 12	2010	124906 (8 pp)	doi :10.1063/1.3415530
12	Reduced electric field in junctionless transistors	JP Colinge et al, Tyndall, ISP-Kiev	2	Applied Phys. Letters	Vol. 96	2010	073510	10.1063/1.3299014
13	Low subthreshold slope in junctionless multigate transistors	JP Colinge et al, Tyndall, ISP-Kiev	2	Applied Phys. Letters	Vol. 96	2010	102106	doi :10.1063/1.3358131
14	Mobility Improvement in Nanowire Junctionless Transistors by Uniaxial Strain	JP Raskin et al, UCL, Tyndall	2, 4	Applied Physics Letters	Vol. 97	2010	042114	doi :10.1063/1.3474608
15	Effect of intravalley acoustic phonon scattering on quantum transport in multigate silicon anowires metal-oxide-semiconductor field-effect transistors	N.D. Akhavan et al, Tyndall, UCL	2, 4	Journal of Applied Physics	Vol. 108	2010	034510	doi :10.1063/1.3457848
16	Random telegraph-signal noise in junctionless transistors	A. Nazarov, ISP-Ukraine, Tyndall	2, 4	Applied Phys. Letters	Vol. 98,	2011	103510.1-3	10.1063/1.3557505
17	Low-frequency noise in junctionless multigate transistors	D. Jang et al INPG, Tyndall	2, 4	Applied Phys. Letters	Vol. 98	2011	p. 133502	doi:10.1063/1.3569724
18	Electrical Properties of LaLuO ₃ /Si(100) Structures Prepared by Molecular Beam Deposition	Yu. Gomeniuk, et al. ISP-Kiev, Tyndall-UCC, AMO, FZJ, Chalmers	1.3	ECS Transactions	33 (3)	2010	pp. 221-227	10.1149/1.3481609
19	Implementation of the symmetric doped double-gate MOSFET model in Verilog-A for circuit simulation	J. Alvarado, et al URV, UCL	4	Int. J. of Numerical Modelling: Electronic Networks, Devices and Fields	Vol 23 (2)	2010	pp. 88-106	10.1002/jnm.725
20	Accurate prediction of the volume inversion impact on undoped Double Gate MOSFET capacitances	O. Moldovan, et al URV, UCL	4	Int. J. of Numerical Modelling: Electronic Networks, Devices and Fields	Vol 23 (6)	2010	pp.447-457	10.1002/jnm.725
21	The equivalent thickness concept for doped symmetric DG MOSFETs	J-M. Sallese et al URV, EPFL	4	IEEE Trans. On Electron Devices	Vol 57 (11)	2010	pp. 2917-2924	10.1109/TED.2010.2071090
22	Why the Universal Mobility Is Not	S. Cristoloveanu, et al UGR, INPG	4	IEEE Trans. On Electron Devices	Vol 57	2010	1327-1333	10.1109/TED.2010.2046109
23	Charging Phenomena at the Interface Between High-k Dielectrics and SiO _x Interlayers	O. Engstrom Chalmers, Livuni, Tyndall, AMO	1.3	J. Telecomm. Inf. Tech.	1	2010	10 – 18	NOT available
24	CV Measurements on LaLuO ₃ Stack MOS Capacitor Using a New 3-Pulse Technique	N. Sedghi LIVUNI, Julich	1.3	J. of Vacuum Scie. And Technology B	Vol. 29, issue 1,	2011	01AB03-1 – 6	10.1116/1.3533267
25	The high-mobility bended n-channel silicon anowires transistor	KE Moselund, et al EPFL, UNEW	2	IEEE Trans. On Electron Devices	vol. 57, no. 4	2010	p. 866-876	10.1109/TED.2010.2040939
26	Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs	M Najmzadeh, et al. EPFL, UNEW	2	Microelectroni c Engineering	vol. 87	2010	pp. 1561-1565	10.1016/j.mee.2009.11.024
27	Strained Si heterojunction bipolar transistor	S Persson et al UNEW, KTH	1	IEEE Trans. On Electron Devices	vol 57,	2010	p. 1243	10.1109/TED.2010.2045667
28	Low-temperature characterization and modeling of advanced GeOI pMOSFETs: Mobility mechanisms and origin of the parasitic conduction	W. Van Den Daele, INPG, CEA/Leti	1, 4	SSE	Vol. 54	2010	pp. 205-212	10.1016/j.sse.2009.12.020
29	Direct measurement of MOSFET channel strain by means of backside etching and Raman spectroscopy on long channel devices	RMB Agaiby, et al UNEW, IMEC	1, 4	IEEE Electron Device Letters	vol. 31, no. 5	2010	pp. 419-421	10.1109/LED.2010.2043496
30	Detailed investigation of effective field, hole mobility and scattering mechanisms in GeOI and Ge pMOSFETs	Van den Daele et al, INPG, Leti, Imec	1, 4	SSE	Vol. 59	2011	pp. 25-33	10.1016/j.sse.2011.01.014

31	Double-gate 1T-DRAM cell using nonvolatile memory function for improved performance	K-H. Park et al, INPG, Korea	4	SSE	Vol. 59	2011	pp. 39-43	10.1016/j.sse.2011.01.007
32	Capacitor-less A-RAM SOI memory: Principles, scaling and expected performance	N. Rodriguez et al INPG, UGR	4	SSE	Vol. 59	2011	pp.44-49	10.1016/j.sse.2011.01.006
ACCEPTED PAPERS – IN PRESS								
1	High hole mobility in 65nm strained Ge-pFETs with HfO ₂ gate dielectric	J. Mitard, et al Warwick, IMEC	1	Japanese Journal of Applied Physics	Accepted Nov 2010,	2011 April		
2	Investigation of strain engineering in FinFETs comprising experimental analysis and numerical simulations	F. Conzatti, et al IUNET, Warwick, IMEC	1, 4	IEEE Trans Electron Devices		Accepted 2010		
3	Erbium silicide growth in the presence of residual oxygen	N. Reckinger, et al UCL, IEMN	1.2	J. Electrochem. Soc.		2011		
4	Transport and Interface States in High-k LaSiOx Dielectric	Yu. Gomeniuk ISP NAS of Ukraine, Tyndall-UCC	1.3	Microelectronics Engineering INFOS'2011		2011	accepted	
5	Studies of the quality of GdSiO-Si interface	M. Iwanowicz (WUT, AMO)	1.3	Microelectronics Reliability	2011 - accepted	2011		
6	A Simplified Physical DC Model for Undoped UTB SOI and Asymmetric DG MOSFETs with Independent Gate Operation	F. Lime, et al URV, Leti	4	Solid-State Electronics	accepted			
7	Investigation of Electron and Hole Charge Trapping in LaLuO ₃ Stack MOS Capacitor Using the 3-Pulse CV Technique	N. Sedghi LIVUNI, Julich	1.3	ECS Transactions	April 2011	2011	In print	
8	A comparative study of surface-roughness induced variability in silicon nanowire and double-gate FETs	INPG/FMNT, IUNET	2, 4	IEEE Trans. on Electron Devices	Special Issue on Variability	2011	7 pages	Not yet available. Accepted

A2.4. Journal publications (only single-partner): 66+8

NO.	Title	Main author, Partners involved	WP/FP	Title of the periodical	Vol., No.	Year	Pages	Permanent identifiers DOI
1	Effect of growth rate on the threading dislocation density in relaxed SiGe buffers grown by reduced pressure chemical vapour deposition at high temperature	A Dobbie, et al Warwick	1	Semiconductor Science and Technology	Vol 25,	2010	085007	10.1088/0268-1242/25/8/085007
2	Highly strained Si epilayers grown on SiGe/Si(100) virtual substrate by Reduced Pressure Chemical Vapour Deposition	M. Myronov, et al Warwick	1	Physica Status Solidi C	Vol 8	2011	pp 952-955	DOI: 10.1002/pssc.201000255
3	Mobility Enhancement in Strained n-FinFETs: Basic Insight and Stress Engineering	N. Serra and D. Esseni; IUNET-Udine	4	IEEE Trans. on Electron Devices	February	2010	482-490	10.1109/TED.2009.2037369
4	An improved empirical approach to introduce quantization effects in the transport direction in multi-subband Monte Carlo simulations	P. Palestri, et al IUNET-Udine	4	Semiconductor Science and Technology	vol. 25, No. 5	2010	055011	10.1088/0268-1242/25/5/055011
5	Simple and efficient modeling of the E-k relationship and low-field mobility in Graphene Nano-Ribbons	M. Bresciani, et al IUNET-Udine	4	Solid-State Electronics	Sept.	2010	1015-1021	10.1016/j.sse.2010.04.038
6	Failure of the Scalar Dielectric Function Approach for the Screening Modeling in Double-Gate SOI MOSFETs and in FinFETs	P. Toniutti, et al IUNET-Udine	4	IEEE Trans. on Electron Devices	Nov.	2010	3074-3083	10.1109/TED.2010.2068990
7	Pseudospectral Methods for the Efficient Simulation of Quantization Effects in Nanoscale MOS Transistors	Alan Paussa et al. IUNET	4	IEEE Trans. on Electron Devices	Dec.	2010	3239-3249	10.1109/TED.2010.2081673
8	Electric Field Control of Spin Rotation in Bilayer Graphene	P. Michetti, et al IUNET Pisa	4, 2	Nano Letters	10,11	2010	4463 – 4469	10.1021/nl102298n
9	Simulation of hydrogenated graphene field-effect transistors through a multiscale approach	G. Fiori, et al IUNET Pisa	4, 2	Phys. Rev. B	82, 15	2010	153404	10.1103/PhysRevB.82.153404
10	Barrier Lowering and Backscattering Extraction in Short-Channel MOSFETs	G. Giusi, et al IUNET	4	IEEE Trans. on Electron Devices	57, 9	2010	2132 – 2137	10.1109/TED.2010.2055273
11	Model and Performance Evaluation of Field-Effect Transistors Based on Epitaxial Graphene on SiC	M. Cheli, P. Michetti, G. Iannaccone IUNET Pisa	4, 2	IEEE Trans. on Electron Devices	57, 8	2010	1936 – 1941	10.1109/TED.2010.2051487
12	Analytical Model of One-Dimensional Carbon-Based Schottky-Barrier Transistors	P. Michetti, G. Iannaccone IUNET Pisa	4, 2	IEEE Trans. on Electron Devices	57, 7	2010	1616 – 1625	10.1109/TED.2010.2049219
13	Statistical Theory of shot noise in quasi-one-dimensional field-effect transistors in the presence of electron-electron interaction	A. Betti, G. Fiori, G. Iannaccone - IUNET Pisa	4	Physical Review B	81, 7	2010	035329	10.1103/PhysRevB.81.035329

14	Model of tunneling transistors based on graphene on SiC	P.Michetti, et al IUNET Pisa	4, 2	Applied Physics Letters	96	2010	133508 – 1/3	10.1063/1.3361657
15	Effects due to backscattering and pseudogap features in graphene nanoribbons with single vacancies	I. Deretzis et al IUNET Pisa	4, 2	Physical Review B	81, 8	2010	085427 – 1/5	10.1103/PhysRevB.81.085427
16	Effective Mobility in Nanowire FETs under Quasi-Ballistic Conditions	E. Gnani, et al IUNET-Bologna	4	IEEE Trans. on Electron Devices	Vol. 57	2010	336 – 343	10.1109/TED.2009.2035545
17	A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs With Different Surface and Channel Orientations—Part I: Fundamental Principles	L. Silvestri, et al IUNET-Bologna	4	IEEE Transactions on Electron Devices	Vol. 57	2010	1567 – 1574	10.1109/TED.2010.2049210
18	A Low-Field Mobility Model for Bulk, Ultrathin Body SOI and Double-Gate n-MOSFETs With Different Surface and Channel Orientations—Part II: Ultra-Thin Silicon Films	L. Silvestri, et al IUNET-Bologna	4	IEEE Transactions on Electron Devices	Vol. 57	2010	1575 – 1582	10.1109/TED.2010.2049211
19	A Low-Field Mobility Model for Bulk and Ultrathin-Body SOI p-MOSFETs With Different Surface and Channel Orientations	L. Silvestri, et al IUNET-Bologna	4	IEEE Transactions on Electron Devices	Vol. 57	2010	3287 – 3294	10.1109/TED.2010.2078821
20	3D simulation of triple-gate MOSFETs with different mobility regions	J. Conde et al, UCL, Mexico, Brazil	4	Microelectronic Engineering	2011	2011		10.1016/j.mee.2011.03.013
21	Realization of ultra dense arrays of vertical silicon NWs with defect free surface and perfect anisotropy using a top-down approach	X-L. Han, et al ISEN-IEMN	2.1	Microelectronic Engineering		2011	on-line 4 january 2011	10.1016/j.mee.2010.12.102
22	Realization of vertical silicon nanowire networks with an ultra high density by top-down approach	X.L. Han, et al ISEN-IEMN	2.1	J. of Nanoscience and Nanotechnology	10	2010	7423-7427	10.1166/jnn.2010.2841
23	Conduction gap in double gate bilayer graphene structure'	V. Hung Nguyen, UPS	2.2	J. Phys.: Condens. Matter	No 22	2010	115304 (6 pages)	10.1088/0953-8984/22/11/115304
24	Negative differential resistance in zigzag-edge graphene nanoribbon junctions	V. Nam Do UPS	2.2	J. Appl. Phys.	No 107	2010	063705 (5 pages)	10.1063/1.3340834
25	Implementation of the Wigner-Boltzmann transport equation within particle Monte Carlo simulation	D. Querlioz, UPS	2 & 4	J. Comput. Electron.	No 9	2010	224-231	10.1007/s10825-009-0281-3
26	Semi-classical and quantum transport in CNTFETs using Monte Carlo simulation	H. Nha Nguyen UPS	2.2, 4	IEEE Trans. Electron Devices	No 58	2011	798-804	10.1109/TED.2010.2096820
27	Electrical characterization of strained and unstrained silicon nanowires with nickel silicide contacts	S. Habicht, FZJ	1.1 & 1.2, 4	Nanotechnology	Vol. 21, No. 10, 2010	2010	105701 (5 pages)	10.1088/0957-4484/21/10/105701
28	Ultrathin Ni Silicides With Low Contact Resistance on Strained and Unstrained Silicon	L. Knoll et al FZJ	1.1 & 1.2	Electron Device Letters	Vol. 31, Issue 4	April 2010	350 - 352	10.1109/LED.2010.2041028
29	Electrical characterization of TbScO ₃ /TiN gate stacks in MOS capacitors and MOSFETs on strained and unstrained SOI	Özben et al FZJ	1.1 & 3	ECS Transactions	Vol.33, No3	2010	195-202	10.1149/1.3481606
30	Formation of steep, low Schottky-barrier contacts by dopant segregation during nickel silicidation	Feste et al FZJ	1.1 & 1.2	Journal of Applied Physics	Vol. 107 Issue 4	Jan. 2010	044510 (6 pages)	10.1063/1.3284089
31	Elastic strain and dopant activation in ion implanted strained Si nanowires	Minamisawa et al FZJ	1.1	J. of Applied Physics	Vol. 108, Issue 12	Dec. 2010	124908 (9 pages)	10.1063/1.3520665
32	Integration of LaLuO ₃ as High-k Dielectric on Strained and Unstrained SOI MOSFETs With a Replacement Gate Process	Özben et al FZJ	1.1 & 1.3 & 3	Electron Device Letters	Vol. 32, Issue 1	Jan. 2011	15-17	10.1109/LED.2011.2089423
33	Rare-earth oxide/TiN gate stacks on high mobility strained silicon on insulator for fully depleted metal-oxide-semiconductor field-effect transistors	Özben et al FZJ	1 & 3	Journal of Vacuum Science & Technology B	Volume 29 / Issue 1	Jan 2011	01A903 -1 to 01A903 -5	10.1116/1.3533760
34	Rare-Earth Scandate/TiN Gate Stacks in SOI MOSFETs Fabricated With a Full Replacement Gate Process	Özben et al FZJ	1.1 & 3	Trans. Electron Devices	Vol. 58, No 3	March 2011	617 - 622	10.1109/TED.2010.2096509
35	Ge quantum dot tunneling diode with room temperature negative differential resistance	M. Oehme, USTUTT	2.4	APPLIED PHYS. LETTERS	Vol 97, Issue 1	2010	012101 (3 pages)	doi:10.1063/1.3462069
36	Multiwavelength micro-Raman analysis of strain in nanopatterned ultrathin strained silicon-on-insulator	O. Moutanabbir, et al USTUTT	1.1 & 1.2	APPLIED PHYS. LETTERS	Vol 97, Issue 5	2010	053105 (3 pages)	doi:10.1063/1.3475399

37	Composition and strain in thin Si _{1-x} Ge _x virtual substrates measured by micro-Raman spectroscopy and x-ray diffraction	T. S. Perova, et al USTUTT	2.4	JOURNAL OF APPLIED PHYSICS	Vol 109, Issue 3 Feb. 2011	2011	033502 (11 pages)	doi:10.1063/1.3536508
38	Lateral electronic transport in 2D arrays of oxidized Si nanocrystals on quartz: Coulomb blockade effect and role of hydrogen passivation	P. Manousiadis, et al NCSR/ IMEL	2.2	Journal of Applied Physics	Twice a month	April 2011	Not known yet	DOI: 1063/1.3575331
39	Nanowire transistors without junctions	JP Colinge et al Tyndall	2	Nature Nanotechnology	Vol. 5, No. 3	2010	225-229	10.1038/NNANO.2010.15
40	LDD and Back-Gate Engineering for Fully Depleted Planar SOI Transistors with Thin Buried Oxide	R. Yan et al , Tyndall	2	IEEE Trans. on Electron Devices	Vol. 57, no 6	2010	1319-1326	10.1109/TED.2010.2046097
41	Variable temperature characterization of low-dimensional effects in tri-gate SOI MOSFETs	C. Barrette et al, Tyndall	2	Solid-State Electronics	Vol. 54	2010	1273-1277	doi:10.1016/j.sse.2010.05.035
42	Junctionless 6T SRAM cell	JP Colinge, Tyndall	2	Electronics Letters	Vol. 46, No. 22	2010	1491-1492	10.1049/el.2010.2736
43	Improvement of carrier ballisticity in junctionless nanowire transistors	N.D.Akhavan et al, Tyndall	2	Applied Phys. Letters	Vol. 98	2011	103510-1-3	doi:10.1063/1.3559625
44	A systematic study of „NH4...2S passivation „22%, 10%, 5%, or 1% on the interface properties of the Al ₂ O ₃ / In _{0.53} Ga _{0.47} As/InP system for n-type and p-type In _{0.53} Ga _{0.47} As epitaxial layers	Eamon O'Connor Tyndall-UCC	1.3	Journal of Applied Physics	109	2011	pp. 024101-1 to 024101-10	10.1063/1.3533959
45	Compact capacitance modeling of a 3-terminal FET at zero drain-source voltage	B. Iñiguez, O. Moldovan URV	4	Solid-State Electronics	vol 54	2010	pp. 520-523	10.1016/j.sse.2009.12.039
46	High-frequency compact analytical noise model of gate-all-around MOSFETs	A. Lázaro, et al URV	2, 4	Semiconductor Science & Technology	Vol. 25 (3)	2010	pp. 035015 (1-10)	10.1088/0268-1242/25/3/035015
47	Analytical Modeling of the Gate Tunneling Leakage for the Determination of Adequate High-K Dielectrics in 22 nm Double-Gate SOI MOSFETs	G. Darbandy et al URV, Cinestav, Mexico	1, 4	Solid-State Electronics	Vol 54 (10)	2010	pp. 1083-1087	10.1016/j.sse.2010.06.015
48	Compact model for long-channel cylindrical surrounding-gate MOSFETs valid from low to high doping concentrations	M. Cheralathan, et al URV, Mexico	2, 4	Solid-State Electronics	Vol. 55 (1)	2011	pp. 13-18	10.1016/j.sse.2010.08.015
49	An analytical model for square GAA MOSFETs including quantum effects	E. Moreno, et al UGR	4	Solid State Electronics	Vol. 54	2010	1463-1469	10.1016/j.sse.2010.05.032
50	Hole transport in DGSOI devices: Orientation and silicon thickness effects	L. Donetti et al UGR	4, 1	Solid State Electronics	Vol 54	2010	191-195	10.1016/j.sse.2009.12.018
51	An in-depth simulation study of Coulomb mobility in ultra-thin-body SOI MOSFETs	F Jimenez-Molinos, et al UGR	4	Semiconductor Science and technology	Vol 25	2010	055002 (8pp)	10.1088/0268-1242/25/5/055002
52	A Model of the Gate Capacitance of Surrounding Gate Transistors: Comparison With Double-Gate MOSFETs	F. Ruiz, et al UGR	4, 1	IEEE Transaction on Electron Devices		2010		10.1109/TED.2010.2058630
53	An Analytical I-V Model for Surrounding-Gate Transistors That Includes Quantum and Velocity Overshoot Effects	J. B. Roldán, et al. UGR	4	IEEE Trans. on Electron Devices	Vol57	2010	2925-2933	10.1109/TED.2010.2067217
54	Simulation of the electrostatic and transport properties of 3D-stacked GAA silicon nanowire FETs	F.G. Ruiz et al UGR	4	Solid State Electronics	Vol 59	2011	62-69	doi:10.1016/j.sse.2011.01.005
55	Multiparameter admittance spectroscopy as a diagnostic tool for interface states at oxide/semiconductor interfaces	B. Raeissi Chalmers	1.3	IEEE Trans. Electron Dev.	35	2010	1702 - 1705	10.1109/TED.2010.2049064
56	Multiparameter admittance spectroscopy	O, Engstrom, et al Chalmers	1.3	ECS Transactions	35(3)	2010	257-	10.1109/TED.2010.2049064
57	Characterization of traps in the transition region at the HfO ₂ /SiO _x interface by thermally stimulated currents	B. Raeissi Chalmers	1.3	J. Electrochem. Soc.	158(3)	2011	G63 - G70	10.1149/1.3530845
58	Suppression of gate-induced drain leakage by optimization of junction profiles in 22 nm and 32 nm SOI nFETs	Andreas Schenk ETHZ	4	Solid-State Electronics	No 54	2010	pp. 115 - 122	doi:10.1016/j.sse.2009.12.005.
59	Linearity and mobility degradation in strained Si MOSFETs with thin gate dielectrics	OM Alatise, et al, UNEW	1, 4	Solid State Electronics	vol. 54, no. 6,	2010	pp. 628-634,	10.1016/j.sse.2009.12.036
60	The impact of self-heating and SiGe strain-relaxed buffer thickness on the analog performance of strained Si nMOSFETs	OM Alatise et al. UNEW	1, 4	Solid State electronics	vol. 54, no. 3,	2010	pp. 327-335	10.1016/j.sse.2009.09.029
61	Statistical-Variability Compact-Modeling Strategies for BSIM4 and PSP	B. Cheng et al, GU	4	IEEE Design & Test of Computers	March Vol. 27, No.2	2010	26-35	10.1109/MDT.2010.53
62	Surface-energy triggered phase formation and epitaxy in nanometer-thick Ni _{1-x} P _x silicide films	J. Luo, et al KTH	1	Applied Physics Letters	96	2010	031911 1-3	10.1063/1.3291679
63	Interaction of NiSi with dopants for metallic source/drain	J. Luo, et al.	1	Journal of	B28	2010	C1 1-11	10.1116/1.32482

	applications	KTH		Vaccum Science Technology				67
64	Analytical modeling of direct tunneling current through gate stacks for the determination of suitable high-k dielectrics for nanoscale double-gate MOSFETs	G. Darbandy, URV, Mexico	1, 4	Semiconductor Science and Technology	Vol. 26 (4)	2011		10.1088/0268-1242/26/4/045002
65	Simulation study of the on-current improvements in Ge and sGe versus Si and sSi nano-MOSFETs	F. Conzatti et al IUNET	4	IEDM	Dec.	2010		
66	Full band assessment of phonon-limited mobility in Graphene NanoRibbons	A. Betti, et al IUNET Pisa	4, 2	Proceeding of the IEDM Tech. Dig.		2010	32.2.1-4	
ACCEPTED PAPERS - IN PRESS								
1	Effect of Ge/Si (001) epilayer thickness on structural quality	V.A. Shah, et al Warwick	1	Thin Solid Films		Acc. In 2010		
2	High quality relaxed Ge layers grown directly on a Si (001) substrate	V.A. Shah, et al Warwick	1	Solid State Electronics		Acc. in 2010		
3	CMOS Inverter based on Schottky Source-Drain MOS Technology with Low Temperature Dopant Segregation	G. Larrieu, E. Dubois (ISEN-IEMN)	1.2	IEEE Electron Dev. Lett.		2011	Accept.	
4	Improvement of immunity on MeV electron radiation of MOS structures by means of ultra-shallow fluorine implantation	M. Kalisz (WUT)	4	Microelectronics Reliability	accepted	2011		
5	Local strained silicon platform based on differential SiGe/Si epitaxy	A. Karmous, USTUTT	2.4	J. of Crystal Growth		2011		
6	Electron states in MOS system	O. Engström Chalmers	1.3	ECS Transaction 2011		2011		
7	Computational Comparison of Conductivity and Mobility Models for Silicon Nanowire Devices	Martin Frey ETHZ	4	Jour. Appl. Phys.	109 (7), Apr.2011	2011		
8	Study of interfaces and band offsets in TiN/amorphous LaLuO ₃ gate stacks	I.Z. Mitrovic LIVUNI	1.3	Microelectron. Engineering	April 2011	2011	In print	

A2.5. Presentation at the Conferences and Workshops (joint): 5 + 52

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/FP	Date	Place
1	Workshop	INPG/FMNT, NCSR	Euro Nano Day	Invited, European Nanoelectronics: the Initiatives and Networks of the Academic Community	1-4	May 2010	Grenoble, France
2	Conference	T. Rudenko et al. ISP-Kiev, UCL	SemOI conference	Invited: Special Features of back-gate the back gate effect in ultra-thin body SOI MOSFETs	4	Oct 25-28, 2010	Kiev, Ukraine
3	Conference	Afzaljan et al. UCL, Tyndall	SemOI conference	Invited: Barrier Resonant Tunneling Transistor: Performance investigation of a Steep Slope, High On-Current device	4	Oct 25-28, 2010	Kiev, Ukraine
4	Conference	O. Engström Chalmers/ITE	INFOS 2011	Invited: Future high-k gate stacks: Report from a tour in the periodic system (Tutorial to be given)	1.3	June 2011	Grenoble
5	Workshop	INPG/FMNT, Warwick, AMO Gmbh, RWTH Aachen, KTH, IUNET, UCL	INC6	Invited: NANOSIL FP7 European Network of Excellence	1-4	May 2010	Grenoble, France
1	Conference	INPG/FMNT, IMEC	ESSDERC'2010	Experimental Analysis of Surface Roughness Scattering in FinFET devices, pp 305-308	4	September 2010,	Sevilla, Spain
2	Conference	L. Donetti, et al Granada, Warwick, KTH	ULIS 2011	On the effective mass of holes in inversion layers	1	Mar 14-16, 2011	Cork, Ireland
3	Conference	E. Simoen, et al Warwick, IMEC	10 th Int. Conf. on Solid-State and Integrated Circuit Technology (IC-SICT 2010)	Low-frequency noise in strained and relaxed Ge pMOSFETs, p891	1	Nov 1-4, (2010)	Shanghai, China
4	Conference	J. Mitard, et al Warwick, IMEC	2010 Int. Conf. on Solid State Devices and Materials (SSDM 2010)	High Hole-Mobility 65nm Biaxially-Strained Ge-pFETs: Fabrication, Analysis and Optimization, p. C-9-2	1	22-24 Sept (2010)	Tokyo, Japan
5	Conference	S.M.Thomas, et al Warwick, Glasgow,	ULIS 2010	Low temperature effective mobility measurements and modelling of high-k gated Si n-MOS and p-MOS	1	17-19 March 2010	Glasgow, UK

		NXP		devices			
6	Conference	Afzaljan et al. UCL, Tyndall	EUROSOI Conference	Variable Barrier Resonant Tunneling Transistor: A New Path Towards Steep Slope and High On-Current?	4	25-27 January 2010	Grenoble, France
7	Conference	Vikram Passi et al. UCL, IEMN, LITEN-CEA	Electrochemical Society Conference - 2011	Functionalization of Silicon Nanowires for Specific Sensing	2	1-May-2011 – 5-May-2011	Montreal, Canada
8	Conference	V. Kilchytska et al. UCL, IMEC	EuroSOI 2010	Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs	4	January 2010	Grenoble, France
9	Conference	M.K.Md Arshad et al. UCL, Leti	ULIS 2010	Improved DIBL in Ultra Thin Body SOI MOSFETs with Ultra Thin Buried Oxide and Inverted Substrate	4	March 2010	Glasgow, UK
10	Conference	V. Kilchytska et al. UCL, IMEC	ESREF 2010	High-energy neutrons effect on strained and non-strained SOI MuGFETs and planar MOSFETs	4	October 2010	Gaeta, Italy
11	Conference	V. Kilchytska et al. UCL, Leti, UNEW	EuroSOI 2011	Ultra-thin body and BOX SOI Analog Figures of Merit	4	January 2011	Granada, Spain
12	Conference	T. Rudenko et al. UCL, ISP-Kiev	EuroSOI 2011	Impact of mobility variation on threshold voltage extraction by transconductance change and gm/Id methods in advanced SOI MOSFETs	4	January 2011	Granada, Spain
13	Conference	V. Kilchytska et al. UCL, Leti	ULIS 2011	High-temperature perspectives of UTB SOI MOSFETs	4	March 2011	Cork, Ireland
14	Conference	T. Rudenko et al. UCL, ISP-Kiev	ULIS 2011	Influence of Drain Voltage on MOSFET Threshold Voltage Determination by Transconductance Change and gm/Id Methods	4	March 2011	Cork, Ireland
15	Conference	S. Makoveev et al. UNEW, UCL, Leti	ULIS 2011	Self-Heating and Substrate Effects in Ultra-Thin Body Ultra-Thin BOX Devices	4	January 2011	Cork, Ireland
16	Conference	V. Passi et al. UCL, ISEN-IEMN	Micro Electro Mechanical Systems Conf., MEMS'2010	Backgate bias and stress level impact on giant piezoresistance effect in thin silicon films and nanowires'	2.1	2010	Hong-Kong
17	Conference	F.M. Bufler, Synopsys, ETHZ, UPS, IUNET	14th International Workshop on Computational Electronics (IWCE 2010)	Comparison of semiclassical transport formulations including quantum corrections for advanced devices with high-k gate stacks, Proc.: p.319-322	4	27-29 October 2010	Pisa, Italy
18	Conference	Turchanikov, V., et al. IMEL, ISP-Kiev	27th International Conference on Microelectronics, MIEL 2010 - Proceedings	"Comparative studies of single- and double-nanocrystal layer NVM structures: Charge accumulation and retention", pp. 103-104	2.2	2010	Nis, Serbia
19	Conference	JP Raskin, UCL, Tyndall	IEEE International SOI Conference	Mobility Improvement in Nanowire Junctionless Transistors by Uniaxial Strain	2	Oct 2010	USA
20	Conference	A. Nazarov, ISP-Ukraine, Tyndall	EUROSOI 2011	Extraction of flat-band voltage and parasitic resistance in junctionless MuGFETs	2	Jan 2011	Spain
21	Conference	Yuri Y. Gomeniuk ISP Kiev, Tyndall-UCC	INFOS 2011	Transport and Interface States in High-k LaSiOx Dielectric	1.3	21 June 2011	Grenoble
22	Conference	Yuri Y. Gomeniuk ISP -Kiev, Tyndall-UCC, KTH, AMO, FZJ	6 th SemOI Conference and 1 st Ukrainian-French Seminar	Electrical properties of high-k LaLuO3 gate oxide for SOI MOSFETs	1.3	24-26 October 2010	Kyiv
23	Conference	Yuri Y. Gomeniuk ISP-Kiev, Tyndall-UCC, AMO, FZJ, Chalmers	ECS-218 (2010)	Electrical Properties of LaLuO3/Si(100) Structures Prepared by Molecular Beam Deposition	1.3	13 October 2010	Las Vegas
24	Conference	Tyndall-UCC, AMO, Jülich	WoDIM 2010	The onset of electrical stress in 3nm and 6nm molecular beam deposited LaLuO3 MOSCAPs on n-Si(100) substrates using a TiN metal gate and an Al back contact	1.3	28-30 th June 2010	Bratislava, Slovakia
25	Conference	M. Balaguer, et al. URV, UGR	EUROSOI	An analytical compact model for Schottky-Barrier Double Gate MOSFETs	1, 4	January 2010	Grenoble (France)
26	Conference	R. Ritzenthaler, et al. URV, CEA/Leti, INPG	EUROSOI	A 2D analytical model of threshold voltage for Pi-gate FinFET transistors	4	January 2010	Grenoble (France)
27	Conference	R. Ritzenthaler, et al. URV, CEA/Leti, INPG	40th European Solid-State Device Research conference (ESSDERC)	3D Analytical Modelling of Subthreshold Characteristics in Pi-gate FinFET Transistors	4	September 2010	Sevilla (Spain)
28	Conference	R. Ritzenthaler et al. URV, CEA/Leti, INPG	IEEE International SOI conference	Parasitic Back-Interface Conduction in Planar and Triple-Gate SOI Transistors	4	2010	San Diego (USA)
29	Conference	R. Ritzenthaler, et al. URV, CEA/Leti, INPG	EUROSOI	A Short-Channel Analytical Model for Triple-gate and Planar FDSOI Transistors	4	2011	Granada (Spain)

30	Conference	M. Cheralathan, et al URV, UGR	EUROSOL	A Compact Double-Gate MOSFET Model Consistent with a MultiSubband Ensemble Monte Carlo Model	4	2011	Granada (Spain)
31	Conference	M. Cheralathan, et al URV, UGR, IUNET	ULIS	Analytical Drain Current Model Reproducing Advanced Transport Models in nanoscale Double-Gate (DG) MOSFETs	4	2011	Cork (Ireland)
32	Conference	B. Raeissi, Chalmers, ITE, AMO, FZ Julich	16 th Workshop on Dielectrics in Microelectronics (Wodim)	Interface state properties of high-k/SiO ₂ /Si interfaces portrayed by multiparameter admittance spectroscopy	1.3	June 28 – 30, 2010	Bratislava
33	Conference	O. Engström Chalmers, INPG, FZJ, AMO	16 th Workshop on Dielectrics in Microelectronics (Wodim)	Capture cross sections for holes at LaLuO ₃ /Si interfaces	1.3	June 28 – 30, 2010	Bratislava
34	Conference	I.Z. Mitrovic et al LIVUNI, Julich	INFOS'2011	Study of interfaces and band offsets in TiN/amorphous LaLuO ₃ gate stacks'	1.3	21-24 June 2011	Grenoble, France
35	Conference	N. Sedghi et al LIVUNI, Julich	219 th ECS Meeting	Investigation of Electron and Hole Charge Trapping in LaLuO ₃ Stack MOS Capacitor Using the 3-Pulse CV Technique	1.3	1-6 May 2011	Montreal, Canada
36	Workshop	N. Sedghi et al LIVUNI, Julich	Wodim 2010	CV Measurements on LaLuO ₃ Stack MOS Capacitor Using a New 3-Pulse Technique	1.3	28-30 June 2010	Bratislava, Slovakia
37	Conference	N. Sedghi/ LIVUNI, Julich	41 st IEEE SISC 2010	Charge Trapping in LaLuO ₃ MOS Capacitors using a New 3-Pulse CV Technique	1.3	December 2010	San Diego, USA
38	Conference	S Makovejev, et al UNEW, UCL	SiRF	RF extraction of self-heating effects in FinFETs of various geometries	4	January 2011	Phoenix, USA
39	Conference	S Makovejev, et al UNEW, UCL	ULIS	Self-heating effect characterisation in SOI FinFETs	4	March 2010	Glasgow, UK
40	Conference	E Escobedo-Cousin et al UNEW, UCL	MRS	Characterizing the effect of uniaxial strain on the surface roughness of Si nanowire MEMS-based microstructures	1, 2, 4	November 2010	Boston, USA
41	conference	E. Sangiorgi et al. IUNET, WUT, GU, UPS,	MIEL conference	Drain Current Computation in Nanoscale nMOSFETs: Comparison of Transport Models	4	May 2010	Serbia
42	Conference	V.Gudmundsson et al. IUNET-Udine and KTH	International Conference on Ultimate Integration	Multi-subband Monte Carlo simulation of fully-depleted silicon-on-insulator Schottky barrier MOSFETs	4, 1	March 2010	UK
43	Conference	M. Schmidt, et al AMO, RWTH	11 th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)	Mobility Extraction in sub 10nm Nanowire nMOSFETs with Gadolinium-Silicate as Gate Dielectric	1.3, 2.1	Feb. 2011	USA
44	Conference	J. Jasiński (WUT, FZJ)	10th ELTE Conference 2010	Influence of annealing temperature on MOSCAPs with LaLuO gate oxide	1.3	2010	Poland
45	Conference	M. Iwanowicz (WUT, AMO)	10th ELTE Conference 2010	Studies of the quality of GdSiO-Si interface	1.3	2010	Poland
46	Conference	I. Ben-Akkez et al INPG, ST, CEA/Leti	ULIS	Characterization and modeling of capacitances in FD-SOI devices	4	2011	Ireland
47	Conference	A.Nazarov et al Tyndall-UCC, ISP-Kiev	ULIS	Extraction of channel mobility in nanowires MOSFETs using Id(Vg) characteristics	2, 4	2011	Ireland
48	Conference	Q. Rafhay, et al. INPG, Cea/Leti	ULIS	Revised approach for the characterization of GIDL	4	2011	Ireland
49	Conference	M. Schmidt, et al FZJ, CEA/Leti	ULIS	Impact of strain and Ge concentration on the performance of planar SiGe band-to-band tunneling transistors	1	2011	Ireland
50	Conference	A. Hubert et al INPG, Leti	ESSDERC	Experimental comparison of programming mechanisms in 1T-DRAM	4	2010	Spain
51	Conference	K. Tachi et al INPG/FMNT, CEA/Leti, ST,	ESSDERC'2010	SD Source/Drain doping optimization in multi-channel MOSFET	4	13-17 September 2010,	Sevilla, Spain
52	Conference	N. Rodrigez, et al. INPG/FMNT, UGR	ESSDERC'2010	Origins of universal mobility violation in SOI MOSFETs	4	13-17 Sept. 2010	Sevilla, Spain

A2.6. Presentation at the Conferences and Workshops (single-partner): 27+81

NO.	Type of activities	Main leader/ author Partners involved	Title of event	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date	Place
1	Conference	INPG/FMNT	French-Ukrainian symposium and SemOI conference	Invited: Elastic and inelastic scattering in SiNWs	2,4, 4	October 2010	Kiev, Ukraine
2	Workshop	INPG/FMNT	Nanosil SiNano Workshop	Invited: Nanowires in the Beyond CMOS and More than Moore perspectives: Electro-mechanical properties	2, 4	17 Sept. 2010	Sevilla, Spain
3	Workshop	INPG/FMNT	Minattec Crossroads	Invited: European Research Roadmap for Nanoelectronics	1-4	June 2010	Grenoble, France
4	Conference	INPG/FMNT	6th International SemOI Conference & 1st Ukrainian-French Seminar on SOI	Invited: Silicon-based devices and materials for nanoscale FETs	1, 2, 4	October 2010	Kiev, Ukraine
5	Conference	INPG/FMNT	4th International Conference on Micro-Nanoelectronics, Nanotechnologies & MEMs	Invited: The Sinano Institute: European Networks and Projects in the fields of More Moore, More than Moore and Beyond-CMOS	1-4	December 2010	Athens, Greece
6	Invited talk	KTH	27th International Conference on Microelectronics (MIEL)	Invited: Nanoscaling of MOSFETs and Implementation of Schottky Barrier S/D contacts	1, 3	16-19 May 2010	NIS, Serbia
7	Invited talk	KTH	18th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)	Invited: Nanoscaled SiGe based MOSFETs	1, 3	2010	Smolenice, Slovakia
8	Invited talk	KTH	10th IEEE International Conference on Solid-State and Integrated Circuit Technology	Invited: Integration of metallic source/drain (MSD) contacts in nanoscaled CMOS technology	1, 3	2010	Shanghai
9	Conference	G. Iannaccone IUNET	European Conference on Nanotechnologies	Invited: Graphene as a material for nanoelectronics (invited - ab #1198)	2, 4	26 April 2010	Vancouver
10	Conference	G. Iannaccone IUNET	SISPAD	Invited: Transport and noise properties of graphene-based transistors revealed through atomistic modelling)	2, 4	6 September 2010	Bologna
11	Conference	V. Kilchytska et al. UCL	SemOI conference	Invited: Effects of high-energy neutrons on advanced SOI MOSFETs	4	Oct 25-28, 2010	Kiev, Ukraine
12	Conference	P. Dollfus, UPS	1st Ukrainian-French Seminar on SOI materials, devices and circuits	Invited: Ohmic and Schottky contact CNTFET: Transport properties and device performance using semi-classical and quantum particle simulation	2,2, 4	24-28 October 2010	Kiev, Ukraine
13	Conference	P. Dollfus, UPS	14th International Workshop on Computational Electronics (IWCE 2010)	Invited: Quantum transport of Dirac fermions in graphene nanostructures, Proc.: p.39-44	2,2, 4	27-29 October 2010	Pisa, Italy
14	Invited lecture	FZJ/ Buca	Seminar Invitation	Invited: From Strained Si to strained Si on Insulator	1.1	08.Nov. 2010	Shanghai China
15	Invited lecture	FZJ/ Mantl	Conference	Invited: High mobility Si-Ge channel and high-k materials for NanoMOSFETs	1, 3	24-May 2010	Stockholm/Sweden
16	Invited lecture	FZJ/ Mantl	Nanosil Workshop		1, 3	13.09. 2010	Seville, Spain
17	Conference	A. G. Nassiopoulou, IMEL	International Conference on Nanomaterials (ICN 2010)	Invited: "Nanostructures on Si by Electrochemistry and their Applications"	2	27-29 April 2010	Kottayam, India
18	Conference	A. G. Nassiopoulou, IMEL	7th International Conference on Porous Semiconductors Science and Technology – PSST 2010	Tutorial: "Porous Si for Electronics and Sensors"	2.2	14-19 March 2010	Valencia, Spain
19	Conference	A. G. Nassiopoulou, IMEL	VCIAN Conference on Interactions Among Nanostructures 2010	Invited: "Photoluminescence from silicon nanocrystal ensembles: effect of exciton migration and role of surface vibration modes"	2.2	21-25 June 2010	Santorini, Greece
20	Conference	JP Colinge, Tyndall	6th International SemOI Workshop on Nanoscaled Semiconductor-on-Insulator Materials, Sensors and Devices	Invited: Junctionless transistors: physics and properties	2	Nov. 2010	Ukraine
21	lecture	R. Mroczynski WUT	12th Polish Seminar "Ion techniques"	Invited: Plasma techniques applications in the technology of non-volatile semiconductor memory (NVSM) devices	1.3	2-5 March 2011	Szklarska Poręba.

							Poland
22	lecture	R. Mroczynski WUT	XII Warsaw Festival of Science	Invited: How the integrated circuit is made...?	1	September 2010	Warsaw
23	Tutorial Course	B. Iñiguez URV	ESSDERC	Invited: Compact Thin-Film SOI MOSFET Modelling	1, 2, 4,	2010	Sevilla (Spain)
24	Tutorial Course	B. Iñiguez URV	TCCM	Invited: Compact Small-Signal FET Modelling	4	2010	Tarragona (Spain)
25	Conference	O. Engström Chalmers	219 ECS Meeting	Invited: Electron states in MOS system (to be presented)	1.3	May 1 – 6, 2011	Montreal
26	Conference	O. Engstrom Chalmers	218 ECS Meeting,	Invited: Multiparameter Admittance Spectroscopy	1.3	Oct. 10 – 15, 2010	Las Vegas
27	Invited lecture	FZJ/ Mantl	International Symposium on Integrated Functionalities	Invited: Ternary high-k oxides for nanoscale logic devices	1, 3	13.06. 2010	Puerto Rico
1	Conference	M. Myronov, et al Warwick,	14th International Conference on Vapor Growth and Epitaxy (ICVGE-14)	Monolayer thickness control during epitaxial growth of high Ge content strained Ge/SiGe multilayers by RP- CVD	1	August 8-13, 2010	Beijing, China
2	Conference	Van Huy Nguyen, et al Warwick,	UK Semiconductors,	Defect Evaluation in Ge and Si _{1-x} Ge _x Epitaxial Layers using an Iodine-Based Selective Etchant	1	July 7-8 (2010)	Sheffiel d, UK
3	Conference	A. Dobbie, et al Warwick,	UK Semiconductors,	Thermal Stability of Strained Ge Layers Grown on Reverse-Graded Si _{0.2} Ge _{0.8} Relaxed Buffers by RP- CVD	1	July 7-8 (2010)	Sheffiel d, UK
4	Conference	V.A. Shah et al. Warwick,	UK Semiconductors,	Thickness studies of high quality Ge layers on Si (001) substrates.	1	July 7-8 (2010)	Sheffiel d, UK
5	Conference	Xue-Chao Liu, et al Warwick,	UK Semiconductors,	Growth and characterization of Ge/Si _{0.4} Ge _{0.6} multiple quantum wells	1	July 7-8 (2010)	Sheffiel d, UK
6	Conference	A. Dobbie, et al Warwick,	E-MRS 2010 Spring Meeting	Relaxation of Strained Germanium Layers Grown on Si _{0.2} Ge _{0.8} Relaxed Buffers by RP-CVD with in-situ H ₂ Annealing	1	June 7- 11, 2010	Strasbo urg, France
7	Conference	M. Myronov, et al. Warwick,	E-MRS 2010 Spring Meeting	Epitaxial growth of Ge layers by RP-CVD using Digermane precursor	1	June 7- 11, 2010	Strasbo urg, France
8	Conference	M. Myronov et al. Warwick,	E-MRS 2010 Spring Meeting	Highly strained Si epilayers grown on SiGe/Si(100) virtual substrates by RP-CVD	1	June 7- 11, 2010	Strasbo urg, France
9	Conference	V.A. Shah, Warwick,	ISTDM 2010	High quality relaxed Ge layers grown directly on a Si (001) substrate.	1	24-26 May 2010	Stockho lm, Sweden
10	Conference	Xue-Chao Liu et al Warwick,	ISTDM 2010	Non-destructive thickness characterization of Si and Ge based heterostructure by x-ray diffraction and reflectivity	1	24-26 May 2010	Stockho lm, Sweden
11	Conference	A. Dobbie et al Warwick,	MRS Spring Meeting	Investigation of the Thermal Stability of Strained Ge Layers by Reduced-Pressure Chemical Vapour Deposition on Relaxed Si _{0.2} Ge _{0.8} Buffers	1	April 5- 9 2010	San Francis co, USA
12	Conference	G. Iannaccone IUNET	International Workshop on Computational Electronics	A multi-scale approach for performance assessment of hydrogenated graphene Field-Effect Transistors	2, 4	28 October 2010	Pisa
13	Conference	A. Betti IUNET	International Workshop on Computational Electronics	Enhanced shot noise in carbon nanotube FETs due to electron-hole interaction	2, 4	28 october 2010	Pisa
14	Conference	V. Bonfiglio IUNET	International Workshop on Computational Electronics	Evaluation of threshold voltage dispersion in 45 nm CMOS technology with TCAD-based sensitivity analysis	4	27 october 2010	Pisa
15	Conference	A. Betti IUNET	IEDM 2010	Full band assessment of phonon-limited mobility in Graphene NanoRibbons,	2, 4	decemb er 2010	San Francis co
16	Conference	Afzaljan et al. UCL	ESSDERC	Breaching the kT/Q Limit with Dopant Segregated Schottky Barrier Resonant Tunneling MOSFETs: a Computational Study	4	Sept. 13-17 2010	Sevilla, Spain
17	Conference	J. Conde at al. UCL, Cinestav- Mexico	MIEL 2010	3D Simulation of Triple-Gate MOSFETs	4	May 2010	Nis, Serbia
18	Conference	I. Garduno et al, UCL, Cinestav- Mexico	MIEL 2010	Modeling of main leakage currents and their contribution to channel current in Fin-FETs	4	May 2010	Nis, Serbia
19	Conference	X.L. Han et al.	European Material Research	Fabrication and electrical characterization of dense	2.1	June	Strasbo

		ISEN-IEMN	Society Spring Meeting	vertical Si nanowires arrays		2010	urg France
20	Conference	X.L. Han ISEN-IEMN	36th International Conference on Micro & Nano Engineering (MNE2010)	Realization of ultra dense arrays of vertical silicon NWs with defect free surface and perfect anisotropy using a top-down approach	2.1	19-22 Sept 2010	Genoa Italy
21	Conference	V. Talbo, UPS	14th International Workshop on Computational Electronics (IWCE 2010)	Fully self-consistent simulation of silicon nanocrystal-based single-electron transistors, Proc.: p. 151-154	2.4	27-29 October 2010	Pisa, Italy
22	Conference	V. Hung Nguyen, UPS	15th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	Quantum transport of Dirac fermions in graphene field effect transistors, Proc.: p. 9-12	2.2	6-8 Septem ber 2010	Bologna , Italy
23	Conference	M. Schmidt, et al AMO	Ultimate Integration on Silicon (ULIS)	Mobility Extraction in sub 10nm Nanowire nMOSFETs with Gadolinium-Silicate as Gate Dielectric	1.3, 2.1	16 March 2011	Cork, Ireland
24	Conference	A. Karmous, USTUTT	Ultimate Integration on Si ULIS2011	Ge Quantum Dot Schottky diode operated in a 89GHz Rectenna / Poster / Proc. pp. 74-76	2.4	March 2011	Cork, Ireland
25	Workshop	E. Kasper, USTUTT	NANOSIL-Workshop Beyond-CMOS	Quantum Structures beyond CMOS / Presentation	2	Februar y 2011	Aachen, German y
26	Conference	H. Xu, USTUTT	The Eleventh Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, SiRF 2011	Integrated W-Band RECTENNA (Rectifying Antenna) with Ge Quantum Dot Schottky Diode/ Presentation	2.4	17-19 January 2011	Phoenix , Arizona, USA
27	Workshop	E. Kasper, USTUTT	5th International Workshop on New Group IV Semiconductor Nanoelectronics	High frequency behaviour of Ge pin junctions / Presentation / Digest of Papers (2010)1-3.	2	29-30 January 2010	Sendai, Japan
28	Conference	S. Gardelis and A. G. Nassiopoulou, IMEL	7th International Conference on Porous Semiconductors Science and Technology – PSST 2010	Colleration of light emission properties with exciton migration in silicon nanocrystal ensembles	2.2	14-19 March 2010	Valenci a, Spain
29	Conference	JP Colinge, Tyndall	EUROSOI Conference	Substrate bias effects in MuGFETs	2	Jan. 2011	Grenob le
30	Conference	JP Colinge, Tyndall	EUROSOI Conference	3D Simulation of RTS Amplitude in Accumulation-Mode and Inversion-Mode Trigate SOI MOSFETs	2, 4	Jan. 2011	Grenob le
31	Conference	JP Colinge, Tyndall	EUROSOI Conference	Comparison of Breakdown Voltage in Bulk and SOI FinFETs	2, 4	Jan. 2010	Grenob le
32	Conference	JP Colinge, Tyndall	WOLTE 9 - Ninth International Workshop on Low Temperature Electronics	Low Temperature Behavior of Junctionless Multiple Gate nMOSFETs	2, 4	Aug 2010	Brazil
33	Conference	JP Colinge, Tyndall	ESSDERC	Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines	2	Sept 2010	Spain
34	Conference	JP Colinge, Tyndall	Solid-State Devices and Materials Conference (SSDM)	Analysis of the Junctionless Transistor Architecture	2	Sept 2010	Japan
35	Conference	JP Colinge, Tyndall	Solid-State Devices and Materials Conference (SSDM)	Short-Channel Junctionless Nanowire Transistors	2	Sept 2010	Japan
36	Conference	JP Colinge, Tyndall	EUROSOI 2011	Comparison of the switching speed in junctionless and accumulation-mode gate-all-around nanowire transistors	2	Jan 2011	Spain
37	Conference	R. T. Doria, USP-Brazil, Tyndall	EUROSOI 2011	Analytical Model for the Threshold Voltage of Junctionless Nanowire Transistors	2, 4	Jan 2011	Spain
38	Conference	JP Colinge, Tyndall	ULIS 2011	Performance Investigation of Short-channel Junctionless Multigate Transistors	2	March 2011	Ireland
39	Conference	Tyndall-UCC	INFOS 2011	Investigation of bulk defects in amorphous and crystalline HfO2 thin films	1.3	21 June 2011	Grenobl e
40	Conference	G. Darbandy, et al, URV	EUROSOI	Analytical Modeling of Direct Tunnelling Current through SiO2/high-k Gate Stacks for the Determination of Suitable High-k Dielectrics for Nanoscale Double-Gate MOSFETs	1, 4	January 2010	Grenobl e (France)
41	Conference	M. Cheralathan, et al URV	ULIS	Compact potential and current model for long-channel doped cylindrical surrounding-gate MOSFETs	2, 4	March 2010	Glasgo w (UK)
42	Conference	M. Schwarz, et al URV	ULIS	2D closed-form model for the source/drain orthogonal electric field in lightly-doped Schottky-Barrier Double-Gate MOSFETs	1, 4	2010	Glasgo w (UK)
43	Conference	M. Schwarz, et al URV	ESSDERC Fringe Poster Session	2D Analytical Calculation of the Tunneling Current in Lightly Doped Schottky Barrier Double-Gate MOSFET	1, 4	2010	Sevilla (Spain)
44	Conference	M. Schwarz, et al URV	MIXDES	Analytical 2D Model for the Channel Electric Field in Undoped Schottky Barrier Double-Gate MOSFET	1, 4	2010	Wrocla w (Poland)

45	Conference	G. Darbandy, et al URV	EUROSOI	Study of Potential High-k Dielectrics for sub 15 nm UTB SOI MOSFETs, Using Analytical Models of the Gate Tunneling Leakage	1, 4	2011	Granada (Spain)
46	Conference	M. Schwarz, et al URV	EUROSOI	2D Analytical Calculation of the Current in Lightly Doped Schottky Barrier DG MOSFET	1, 4	2011	Granada (Spain)
47	Conference	T. Holtij, et al URV	ULIS	2D Analytical Calculation of the Source/Drain Access Resistance in DG-MOSFET Structures	4	2011	Cork (Ireland)
48	Conference	M. Schwarz, et al URV	ULIS	2D Analysis of Source/Drain Carrier Tunneling in Lightly Doped Schottky Barrier DG-MOSFETs Using a Fully Analytical Model	4	2011	Cork (Ireland)
49	Conference	UGR Jose Luis Padilla, Francisco Gamiz	ULIS-2010	Barrier lowering implementation in SB-MOSFETs on SOI substrates	1, 4	16-18 March	Glasgow
50	Conference	UGR Carlos Sampedro, Francisco Gamiz et al.	ULIS-2010	Channel Length impact on Velocity Overshoot in UTB-DGSOI	4	16-18 March	Glasgow
51	Conference	R Kapoor, et al UNEW	ESREF	Characterising gate dielectrics in high mobility devices using novel nanoscale techniques	1, 4	October 2010	Italy
52	conference	A. Asenov et al., GU	Custom Integrated Circuits Conference (CICC), 2010 IEEE	Modeling and Simulation of Transistor and Circuit Variability and Reliability	4	Sept. 2010	USA
53	Conference	A. Asenoc et al., GU	Design, Automation & Test in Europe Conference & Exhibition (DATE), 2010	Capturing Intrinsic Parameter Fluctuations using the PSP Compact Model	4	March 2010	Dresden
54	Conference	A. Paussa et al. IUNET-Udine	International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	Pseudo-Spectral Method for the Modelling of Quantization Effects in Nanoscale MOS Transistors	4	March 2010	UK
55	Conference	P.Toniutti, et al IUNET-Udine	International Conference on Ultimate Integration on Silicon (ULIS)	Understanding the mobility reduction in MOSFETs featuring high-k dielectrics	4	March 2010	UK
56	Conference	A. Betti, G. Fiori, G.Iannaccone IUNET Pisa	IEDM Tech. Dig.	Full band assessment of phonon-limited mobility in Graphene NanoRibbons	4	Dec. 2010	USA
57	Conference	A. Betti G. Fiori, G. Iannaccone - IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	Enhanced shot noise in carbon nanotube FETs due to electron-hole interaction	4	Oct. 2010	Pisa, Italy
58	Conference	G. Giusi, G. Iannaccone, D. Maji, F. Crupi - IUNET Pisa	10th IEEE International Conference on Solid-State and Integrated Circuit Technology (CSICT-2010)	Experimental extraction of barrier lowering and backscattering in saturated short-channel MOSFETs	4	Nov. 2010	
59	Conference	G. Iannaccone, A. Betti, G. Fiori - IUNET Pisa	International Conference on Simulation of Semiconductor Processes and Devices, (SISPAD)	Transport and noise properties of graphene-based transistors revealed through atomistic modeling	2, 4	March 2010	Italy
60	Conference	G. Fiori, et al IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	A multi-scale approach for performance assessment of hydrogenated graphene Field-Effect Transistors	2, 4	Oct. 2010	Pisa, Italy
61	Conference	V. Bonfiglio, G. Iannaccone - IUNET Pisa	14th International Workshop on Computational Electronics, (IWCE 2010)	Evaluation of threshold voltage dispersion in 45 nm CMOS technology with TCAD-based sensitivity analysis	4	Oct. 2010	Pisa, Italy
62	Conference	L. Silvestri, et al IUNET-Bologna	International Conference on Ultimate Integration on Silicon (ULIS)	Mobility Model for Electrons and Holes in FinFETs with High-k Stacks, Metal Gate and Stress	4	March 2010	UK
63	Conference	A.T. Pham, TUBS	IWCE	Simulation of Landau quantization effects due to strong magnetic fields in (110) Si hole inversion layers	4	Oct. 2010	Pisa, Italy
64	Conference	A.T. Pham, TUBS	ESSDERC	Comparison of Strained SiGe Heterostructure on Insulator (001) and (110) PMOSFETs: C-V Characteristics, Mobility, and ON current	4	Sept. 2010	Spain
65	Conference	H. Xu, USTUTT	11 th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)	Integrated W-band RECTENNA (rectifying antenna) with Ge quantum dot Schottky Diode	2.4	Feb. 2011	USA
66	Conference	M. Iwanowicz (WUT)	10th ELTE Conference 2010	Vector generator for pulse characterization of MOS devices	1.3	2010	Poland
67	Conference	J. Jasiński (WUT)	10th ELTE Conference 2010	Electrical characterization of MOSFETs with HfSiON gate	1.3	2010	Poland
68	Conference	R. Mroczyrński (WUT)	WoDiM 2010	Reliability issues of double gate dielectric stacks based on hafnium dioxide (HfO ₂) layers for non-volatile semiconductor memory (NVSM) applications	1.3	2010	Bratislava, Slovakia
69	Conference	M. Kalisz (WUT)	5 th Wide Bandgap Materials -	Effect of the Fluorine Implantation from r.f. CF ₄ plasma	1.3	2010	Poland

			progress in synthesis and applications and 7 th Diamond & Related Films jointly with 2 nd International Workshop on Science and Applications of Nanoscale Diamond Materials, Zakopane, Poland	on Electrical Characteristics of MIS Structures with PECVD Silicon Oxynitride Layers			
70	Conference	M. Kalisz (WUT)	10 th Conference "Electron Technology", ELTE 2010, Wroclaw, Poland	Improvement of immunity on MeV electron radiation of MOS structures by means of ultra-shallow fluorine implantation	1,3	2010	Poland
71	Conference	E. Gnani et al IUNET	ULIS 2011	Numerical Investigation on the Junctionless Nanowire FET	2,4	2011	Ireland
72	Conference	L. Knoll et al FZJ	ULIS 2011	20 nm gate length Schottky MOSFETs with ultra thin NiSi/epitaxial NiSi ₂ source/drain	1	2011	Ireland
73	Conference	A. Martinez UG	ULIS	NEGF simulations of a junctionless Si gate-all-around nanowires transistor with discrete dopants	2,4	2011	Ireland
74	Conference	A. Kranti et al UCL	ULIS	Source/Drain engineering ultra low power analog/RF UTBB MOSFETs	4	2011	Ireland
75	Conference	J. El Hussein et al URV, IES Montpellier	ULIS	A surface potential based compact model for lightly doped FD SOI MOSFETs with ultra-thin body	4	2011	Ireland
76	Conference	A. Nichau et al FZJ	ULIS	Lanthanum Lutetium oxide integration in a gate-first process on SOI MOSFETs	1	2011	Ireland
77	Conference	X. Wand, et al GU	ULIS	Channel length dependence of statistical threshold voltage variability in extremely scaled HKMG MOSFETs	4	2011	Ireland
78	Conference	C. Sampedro et al UGR	ESSDERC	Multi-subband Monte Carlo Simulation of bulk MOSFETs for the 32nm-Node and beyond	4	2010	Spain
79	Conference	S.Narasimhamoorthy et al INPG/FMNT	ESSDERC'2010	Parameter extraction of nanoscale MOSFETs using modified Y function method	4	September 2010,	Sevilla, Spain
80	Conference	K. Boucart, et al. EPFL	ESSDERC'2010	A simulation-based study of sensitivity to parameter fluctuations of Si tunnel FETs	2,4	September 2010,	Sevilla, Spain
81	Conference	S. Habicht, et al FZJ	ESSDERC'2010	Hole mobilities and electrical characteristics of omega-gated silicon nanowires array FETs with 110- and 100-channel orientation	2,4	September 2010,	Sevilla, Spain

A2.7. Other dissemination actions (joint): 3

NO.	Type of activities	Main leader/ author Partners involved	Title of paper/presentation/etc.	WP/ FP	Date
1	Web site	Sinano Institute, -Grenoble INP, -UCL	Nanosil Project, regular update	All	2010-11
2	Film	Sinano Institute, Grenoble INP, KTH, IUNET, UCL	Sinano Institute	All	2011
3	News Letter	UCL, Sinano Institute, Grenoble INP, IEMN, FZJ, Warwick, KTH, USTUTT, AMO, RWTH, IUNET, Chalmers, EPFL	Nanosil News Letter 2009	All	2010

A2.8. Other dissemination actions (single-partner): 4

NO.	Type of activities	Main leader/ author Partners involved	Title of paper/presentation/etc. Emphasize if invited	WP/ FP	Date	Place
1	Thesis	N. Reckinger UCL	Fabrication and characterization of rare-earth silicide thin films	1.2	11.02. 2011	Louvain-la-Neuve
2	Thesis	B. Raeissi Chalmers	Charge carrier traffic at interfaces in nanoelectronic structures, ISSN 1652-0769, 2010	1.3	2010	
3	Thesis	ETHZ	Scattering in Nanoscale Devices	4	2010	Zurich
4	Thesis	ETHZ	Band Structure Effects and Quantum Transport	4	2010	Zurich