

104 papers (see lists of joint and single-partner papers separately) in high-level international journals have been prepared by Nanosil members in 2009, among which **77** articles are already published, **12** are accepted for publication in 2009 and **15** are submitted. **45** of them are **joint papers** (i.e. almost half), among which **36** articles are already published, **4** are accepted for publication in 2009 and **5** are submitted. Here we included only journal publications (+IEMD top conference), while the numbers would have been well greater if we would take into account publications in conference proceedings (which follow almost all conferences listed below). Only publications clearly acknowledging Nanosil are listed.

142 conference/workshop presentations (see list of references) have been given by Nanosil partners in 2009 (and accepted for 2010), among which **36 are invited presentations**. **43** and **8** of them, respectively, are **joint** presentations.

References

Journal publications (only joint)

Title	Authors	Nanosil partners	WP	References (journal, vol. ??, No. ??, pp. ??-??)	Status (published/accepted/submitted)
Ultra compact FDSOI transistors including strain and orientation : processing and performance	C. Fenouillet-Beranger, L. Pham Nguyen, P. Perreau, S. Denorme, F. Andrieu, O. Faynot, L. Tosti, L. Brevard, C. Buj, O. Weber, C. Gallon, V. Fiori, F. Boeuf, S. Cristoloveanu, T. Skotnicki	INPG-FMNT, CEA-LETI	4	ECS Transactions, 19, n± 4, 55–64 (2009)	published
Floating-body SOI memory: concepts, physics and challenges	M. Bawedin, S. Cristoloveanu, D. Flandre, F. Udrea	INPG-FMNT, UCL	4	ECS Transactions, 19, n± 4, 243–256 (2009)	published
Low-temperature measurements on Germanium-on-Insulator pMOSFETs: evaluation of the background doping level and modeling of the threshold voltage dependence	W. Van Den Daele, E. Augendre, K. Romanjek, C. Le Roeyr, L. Clavelier, J-F. Damlencourt, E. Guiot, B. Ghyselen, S. Cristoloveanu	INPG-FMNT, CEA-LETI	4	ECS Transactions, 19, n± 4, 145–152 (2009)	published
Low-temperature characterization and modeling of advanced GeOI pMOSFETs: mobility mechanisms and origin of the parasitic conduction	W. Van Den Daele, E. Augendre, C. Le Royer, J.-F. Damlencourt, B. Grandchamp, S. Cristoloveanu	INPG-FMNT, CEA-LETI	4	Solid State Electronics	in press, DOI
DC and Low Frequency Noise Characterization of FinFET Devices	K. Bennamane, T. Boutchacha, G. Ghibaudo, M. Mouis, N. Collaert	INPG-FMNT, IMEC	4	Solid State Electronics, 53, 1263–1267 (2009)	published
Piezoresistance Effect of Strained and Unstrained Fully-Depleted Silicon-On-Insulator MOSFETs Integrating an HfO ₂ /TiN Gate Stack	F. Rochette, M. Cassé, M. Mouis, A. Haziot, T. Pioger, G. Ghibaudo, F. Boulanger	INPG-FMNT, CEA/LETI	4	Solid-State Electronics, Volume 53, Issue 3, Pages 392-396 (March 2009)	published

A comprehensive study of magnetoresistance mobility in short channel transistors: Application to strained and unstrained silicon-on-insulator field-effect transistors	M. Cassé, F. Rochette, L. Thévenod, N. Bhouri, F. Andrieu, G. Reimbold, F. Boulanger, M. Mouis, G. Ghibaudo, D.K. Maude	INPG-FMNT, CEA/LETI	4	Journal of Applied Physics, J. Appl. Phys. Vol. 105, pp. 084503 (April 2009)	published
Strain sensitivity of gate leakage in strained-SOI nMOSFETs: a benefit for the performance trade-off and a novel way to extract the strain-induced band offset	F. Rochette, X. Garros, G. Reimbold, F. Andrieu, M. Cassé, M. Mouis, G. Ghibaudo and F. Boulanger	INPG-FMNT, CEA/LETI	1	Microelectronic Engineering, Volume 86, Issues 7-9, pp. 1897-1900 (July-Sept. 2009)	in press, DOI
Full quantum treatment of surface roughness effects in Silicon nanowire and double gate FETs	M.G. Pala, C. Buran, S. Poli, and M. Mouis	FMNT-INPG, IUNET	2	J. Comp. Electronics Vol. 8, no. 3, p. 374-381 (Oct. 2009)	published
Channel-Length Dependence of Low-Field Mobility in Silicon-Nanowire FETs	S. Poli, M.G. Pala	FMNT-INPG, IUNET	2	IEEE Electron Devices Letters Vol. 30, no. 11, pp. 1212-1214 (2009)	published
Phonon- and surface-roughness-limited mobility of gate-all-around 3C-SiC and Si nanowire FETs	K. Rogdakis, S. Poli, E. Bano, K. Zekentes, M.G. Pala	FMNT-INPG, IUNET	2	Nanotechnology Vol. 20 no. 29, p. 295202 (2009)	published
Full Quantum Treatment of Remote Coulomb Scattering in Silicon Nanowire FETs	S. Poli, M.G. Pala, T. Poiroux	FMNT-INPG, IUNET	2	IEEE Trans. Electron Devices Vol. 56, no. 6, pp. 1191-1198 (2009)	published
Improved effective mobility extraction in MOSFETs	S.M. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, R.J.P. Lander, G. Vellianitis and J.R. Watling	Warwick, Glasgow	1	Solid-State Electronics, 53, 1252-1256 (2009)	published
Experimental and physics based modeling assessment of strain induced mobility enhancement in FinFETs	N.Serra, F.Conzatti, D.Esseni, M.De Michielis, P.Palestri, L.Selmi, S.Thomas, T.E.Whall, E.H.C.Parker, D.R.Leadley, L. Witters, A.Hikavy, M.J.Hýtch, F.Houdellier, E.Snoeck, T.J.Wang, W.C.Lee, G.Vellianitis, M.J.H.van Dal, B.Duriez, G.Doornbos and R.J.P.Lander	IUNET, Warwick,	1, 4	IEDM Tech Dig. 4.2 (2009)	published
Schottky barrier lowering with the formation of crystalline Er silicide on n-Si upon thermal annealing	N. Reckinger, X. Tang, V. Bayot, D. A. Yarekha, E. Dubois, S. Godey, X. Wallart, G. Larrieu, A. Łaszcz, J. Ratajczak, P. J. Jacques, J.-P. Raskin	UCL IEMN	2	APPLIED PHYSICS LETTERS 94, 191913 (2009)	published
Substrate impact on threshold voltage and subthreshold slope of sub-32 nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel, Solid-State Electronics	S. Burignat, D. Flandre, M.K. Md Arshad, V. Kilchytyska, F. Andrieu, O. Faynot and J.-P. Raskin	UCL CEA-LETI	4	Solid State Electronics, No. 12, 2009	in press, DOI

Experimental study of transconductance and mobility behaviors in ultra-thin SOI MOSFETs with standard and thin buried oxides	T. Rudenko, V. Kilchytska, S. Burignat, J.-P. Raskin, F. Andrieu, O. Faynot, Y. Le Tiec, K. Landry, A. Nazarov, V.S. Lysenko, D. Flandre	ISP-Kiev, UCL, CEA-LETI	4	Solid State Electronics, No. 12, 2009	in press, DOI
An electrical evaluation method for the silicidation of silicon nanowires	X. Tang, N. Reckinger, V. Bayot, D. Flandre, E. Dubois, D. A. Yarekha, G. Larrieu, A. Lecestre, J. Ratajczak, N. Breil, V. Passi, and J.-P. Raskin	UCL, IEMN	2	APPLIED PHYSICS LETTERS 95, 023106 2009	published
Arsenic-Segregated Rare Earth Silicide Junctions: Reduction of Schottky Barrier and Integration in Metallic n-MOSFETs on SOI	G. Larrieu, D. Yarekha, E. Dubois, N. Breil, O. Fainot	ISEN-IEMN LETI	1	IEEE Electron Device Letters, vol.30, n°11 pp. 1266-1268, December 2009	published
Issues associated to rare earth silicide integration in ultra thin FD SOI Schottky barrier nMOSFETs	G. Larrieu, D. Yarekha, E. Dubois, N. Breil, N. Reckinger, X. Tang and A. Halimaoui	ISEN-IEMN UCL ST	1	'Silicon-on-Insulator Technology and Devices 14' ECS transactions, vol. 19, n° 4, pp 201-207, 2009	published
UHV Fabrication of the Ytterbium Silicide as Potential low Schottky Barrier S/D Contact Material for n-type MOSFET	D. Yarekha, G. Larrieu, N. Breil, E. Dubois, S. Godey, X. Wallart, C. Soyer, D. Remiens, N. Reckinger, X. Tang, A. Laszcz, J. Ratajczak and A. Halimaoui	ISEN-IEMN UCL ST	1	'Silicon-on-Insulator Technology and Devices 14' ECS transactions, vol. 19, n° 4, pp 339-344, 2009	published
RF performance of valence band-edge metallic S/D junctions in SOI MOSFETs via dopant segregation engineering	R. Valentin, E. Dubois, G. Larrieu, N. Breil, J.P. Raskin, G. Dambrine, F. Danneville	ISEN-IEMN UCL ST	1	IEEE Electron Device Letters, vol.30, n°11 pp. 1197-1199, November 2009.	published
Nanosil Network of Excellence Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications	F. Balestra, E. Parker, D. Leadley, S. Mantl, E. Dubois, O. Engstrom, R. Clerc, S. Cristoloveanu, H. Kurz, J.P. Raskin, M. Lemme, A. Ionescu, E. Kasper, A. Karmous, M. Baus, B. Spangenberg, M. Ostling, E. Sangiorgi, G. Ghibaudo, D. Flandre	ISEN-IEMN UCL ST	1	Materials Science in Semiconductor Processing, Volume 11, Issue 5, October 2009, pages 148-159	published invited
Mobility Extraction in SOI MOSFETs with sub 1 nm Body Thickness	M. Schmidt, M.C. Lemme, H.D.B. Gottlob, H. Kurz, F. Driussi, L. Selmi	AMO, IU.NET	3, 4	Solid-State Electron. 53(12), pp. 1246–1251. Dec. 2009	published
Scaling potential and MOSFET integration of thermally stable Gd silicate dielectrics	H.D.B. Gottlob, M. Schmidt, A. Stefani, M.C. Lemme, H. Kurz, I.Z. Mitrovic, W.M. Davey, S. Hall, M. Werner, P.R. Chalker, K. Cherkaoui, P.K. Hurley, J. Piscator, O. Engström, S.B. Newcomb	AMO, LIVUNI, Tyndall-UCC, Chalmers	1	Microelectron. Eng., 86(7-9), pp. 1642-1645, 2009	published

Leakage current effects on C-V plots of high-k MOS capacitors	Y. Lu, S. Hall, L. Z. Tan, I. Z. Mitrovic, W. M. Davey, B. Raeissi, O. Engström, K. Cherkaoui, S. Monaghan, P. K. Hurley, H.D.B. Gottlob, M.C. Lemme	LIVUNI, Tyndall-UCC, Chalmers, AMO	1	J. Vac. Sci. Technol. B, 27(1), pp. 352-355, Jan./Feb. 2009	published
Analysis of electron mobility in HfO ₂ /TiN gate metal-oxide-semiconductor field effect transistors: The influence of HfO ₂ thickness, temperature, and oxide charge	M. A. Negara, K. Cherkaoui, P. K. Hurley, C. D. Young, P. Majhi, W. Tsai, D. Bauza and G. Ghibaudo,	Tyndall Institute, INTEL and IMEP	1 and 4	J. Appl. Phys. 105, 024510 (2009)	published Ackn. Sinano
Direct protein detection with a nano-interdigitated array gate MOSFET	X. Tang, A. M. Jonas, B. Nysten, S. Demoustier-Champagne, F. Blondeau, P. Prevot, R. Pampin, E. Godfroid, B. Iñiguez, J. P. Colinge, J. P. Raskin, D. Flandre, V. Bayot	UCL, URV, Tyndall	3,4	Biosensors & Bioelectronics Volume: 24 Issue: 12 Pages: 3531-3537 Published: AUG 15 2009	published
Implementation of the symmetric doped double-gate MOSFET model in Verilog-A for circuit simulation	J. Alvarado, B. Iñiguez, M. Estrada, D. Flandre, A. Cerdeira	URV, UCL	4	International Journal of Numerical Modelling: Electronic Networks, Devices and Fields	in press
Non-metallic effects in silicided gate MOSFETs	N.Rodriguez, F.Gamiz, R.Clerc, C.Sampedro, G.Ghibaudo, A.Godoy	UGR, INPG	4	Solid State Electronics, 53, pp. 1313-1317	published
Confind energy states in semiconductors detected by a resonant differential capacitance method	O. Engström, M. Kaniewska, M. Kracsmarczyk	Chalmers, ITE	2	<i>Appl. Phys. Lett.</i> 95 , 013104 (2009)	published
Charging phenomena at the interface between high-k dielectrics and SiO _x interlayers	O. Engström, B. Raeissi, J. Piscator, I.Z. Mitrovic, S. Hall, H.D.B. Gottlob, M. Schmidt, P.K. Hurley, K. Cherkaoui	Chalmers, Liverpool, AMO, Tyndall	1	<i>J. Telecom. Inf. Tech.</i> , No. 4, 2009	in press
Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs	M. Najmzadeh, L. De Michielis, D. Bouvet, P. Dobrosz, S. Olsen, A.M. Ionescu	EPFL/ UNEW	1&2	Microelectronic Eng.	in press, DOI
Nanoscale strain characterisation for ultimate CMOS and beyond	SH Olsen, P Dobrosz, RMB Agaiby, YL Tsang, O Alatise, SJ Bull, AG O'Neill, KE Moselund, AM Ionescu, P Majhi, D Buca, S Mantl and H Coulson	UNEW, EPFL, FZJ	1&4	Materials Science in Semiconductor Processing, vol. 11, no. 5-6, pp. 271-278, 2009	published
Strained Si/SiGe MOS technology: improving gate dielectric integrity	SH Olsen, L Yan, R Agaiby, E Escobedo-Cousin, AG O'Neill, PE Hellstrom, M Ostling, K Lyutovich, E Kasper, C Claeys and EHC Parker	UNEW, KTH, USTUTT, WARWICK	1	Microelectronic Engineering, vol. 86, pp. 218-223, 2009	published

Investigation of oxidation-induced strain in a top-down Si nanowire platform	M Najmzadeh, D Bouvet, P Dobrosz, SH Olsen and A Ionescu	UNEW, EPFL	2&4	Microelectronic Engineering, vol. 86, no. 7-9, pp. 1961-1964, 2009	published
TEM analysis of Ge-on-Si MOSFET structures with HfO ₂ dielectric for high performance PMOS device technology	DJ Norris, T Walther, AG Cullis, M Myronov, A Dobbie, T Whall, EHC Parker, DR Leadley, B De Jaeger, W Lee, M Meuris, J Watling and A Asenov	Warwick, IMEC, Glasgow	1, 4	Journal of Physics: Conference Series	accepted
Reduced Electric Field in Junctionless Transistors	J.-P. Colinge, C.-W. Lee, I. Ferain, N. Dehdashti Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, R. T. Doria	Tyndall, Inst. Semicond. Phys, Kiev	2	Appl. Phys. Lett.	accepted
Accurate prediction of the volume inversion impact on undoped Double Gate MOSFET capacitances	O. Moldovan, F. A. Chaves, D. Jiménez, J.-P. Raskin and B. Iñiguez	URV, UCL	4	International Journal of Numerical Modelling: Electronic Networks, Devices and Fields	accepted
Classification of energy levels in quantum dot structures by means of depleted layer spectroscopy methods	M.Kaniewska, O. Engström, M. Kaczmarczyk	ITE, Chalmers	2	<i>J. Mat. Sci.</i> , 2010	accepted
Why the Universal Mobility is not	S. Cristoloveanu, N. Rodriguez, F. Gamiz	UGR, INPG/FMNT	4	IEEE Transactions on Electron Devices	submitted
Small-Signal Analysis of High-Performance p- and n-type SOI SB-MOSFETs with Dopant Segregation	C. Urban, M. Emam, C. Sandow, Q. T. Zhao, A. Fox, S. Mantl, J.-P. Raskin	UCL, FZJ	1, 4	Solid State Electronics	submitted
Radio frequency study of dopant-segregated n-type SBMOSFETs on thin-body SOI	C. Urban, M. Emam, C. Sandow, J. Knoch, Q.-T. Zhao, J.-P. Raskin, S. Mantl	UCL, FZJ	1, 4	IEEE Electron Device Letters	submitted
Low Subthreshold Slope in Junctionless Multigate Transistors	C.-W. Lee, A. N. Nazarov, I. Ferain, N. Dehdashti Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, J.-P. Colinge	Tyndall, Institute of Semiconductor Physics, Kiev,	2	Applied Phys. Lett.	submitted
A quasi-analytical model for Nanowire FETs with arbitrary polygonal cross section	L. De Michielisa, L. Selmib, A. M. Ionescu	EPFL, IUNET	2, 4	Solid State Electronics	submitted

Journal publications (only single-partner)

Title	Authors	Nanosil partners	WP	References (journal, vol. ??, No. ??, pp. ??-??)	Status (published/accepted/ submitted)
Multi-gate Devices for High Performance, Ultra Low Power and Memory applications	F. Balestra	INPG-FMNT	1,2,4	Invited paper, ECS Transactions, Volume 25, Issue 7 "ULSI Process Integration", pp. 77-90, 2009	published

Three-Dimensional Real-Space Simulation of Surface Roughness in Silicon Nanowire FETs	C. Buran, M.G. Pala, M. Bescond, M. Dubois, and M. Mouis	FMNT-INPG	2	IEEE Trans. Electron Devices Vol. 56, no. 10, pp. 2186-2192 (Oct. 2009)	published
Effects of Carbon on Schottky Barrier Heights of NiSi Modified by Dopant Segregation	J. Luo, Z.J. Qiu, D.W. Zhang, P.-E. Hellström, M. Östling and S.-L. Zhang	KTH	1	IEEE Electron Device Letters 30, 608(2009)	published
Fully Depleted UTB and Trigate N-Channel MOSFETs Featuring Low-Temperature PtSi Schottky-Barrier Contacts With Dopant Segregation	V. Gudmundsson, P.-E. Hellström, J. Luo, J. Lu, S.-L. Zhang and M. Östling,	KTH	1	IEEE Electron Device Letters 30, 541(2009).	published
"Perspectives of graphene nanoelectronics: probing technological options with modeling"	G. Iannaccone, G. Fiori, M. Macucci, P. Michetti, M. Cheli, A. Betti, P. Marconcini	IUNET	2	IEDM, pp.245-248, 2009.	published
"Physical insights on graphene nanoribbon mobility through atomistic simulations"	A. Betti, G. Fiori, G. Iannaccone	IUNET	2	IEDM, pp.897-900, 2009	published
"Ultralow-Voltage Bilayer Graphene Tunnel FET"	G. Fiori, G. Iannaccone	IUNET	2	IEEE Electron Device Letters, 30, 10, pp.1096-1098 (2009)	published
"Shot Noise Suppression in Quasi-One-Dimensional Field-Effect Transistors"	A. Betti, G. Fiori, G. Iannaccone	IUNET	2	IEEE Trans. Electron Devices, 56, 9, pp.2137-2143 (2009)	published
"On the Possibility of Tunable-Gap Bilayer Graphene FET"	G. Fiori, G. Iannaccone	IUNET	2	IEEE Electron Device Letters, 30, 3, pp.261 – 264 (2009)	published
"Analytical Model of Nanowire FETs in a Partially Ballistic or Dissipative Transport Regime"	P. Michetti, G. Mugnaini, G. Iannaccone	IUNET	4	IEEE Transaction Electron Devices, 56, 7, pp.1402 – 1410 (2009)	published
"A Semianalytical Model of Bilayer-Graphene Field-Effect Transistor"	M. Cheli, G. Fiori, G. Iannaccone	IUNET	4	IEEE Trans. Electron Devices, Vol. 56, pp. 2979-2986, 2009	published
Semiclassical Modeling of Quasi-Ballistic Hole	M. De Michielis, D. Esseni, P.Palestri, L. Selmi	IUNET-UD	4	IEEE Transactions on Electron Devices, n. 9, vol. 56, Sept. 2009, pp. 2081-2091	published
Simulation Study of Coulomb Mobility in Strained Silicon	F. Driussi and D. Esseni	IUNET-UD	4	IEEE Transactions on Electron Devices, Vol.56, NO.9, pp.2052-2059, Sept. 2009	published
Theory of the Motion at the band crossing points in bulk semiconductor crystals and in inversion layers	D. Esseni, P Palestri	IUNET-UD	4	Journal of Applied Physics, vol. 105, no. 5, march 2009, p. 053702-1 - 053702-11	published
Multi-Subband Monte Carlo simulations of ION degradation due to fin thickness fluctuations in FinFETs	N. Serra, P. Palestri, G.D.J. Smit, L. Selmi	IUNET-UD	4	Solid-State Electronics, vol. 53, febbraio 2009, pp. 424-432	published

Drain current improvements in uniaxially strained p-MOSFETs: A Multi-Subband Monte Carlo study	F. Conzatti, M. De Michielis, D. Esseni, P. Palestri	IUNET-UD	4	Solid-State Electronics, vol. 53, maggio 2009, pag. 706-711	published
Multiscale simulation of carbon nanotube devices	C. Adessi, R. Avriker, X. Blase, A. Bournel, H. Cazin d'Honinchtun, P. Dollfus, S. Frégonèse, S. Galdin-Retailleau, A. López-Bezanilla, C. Maneux, H. Nha Nguyen, D. Querlioz, S. Roche, F. Triozon, T. Zimmer	UPS	2	C. R. Phys. 10 (2009) 305-319	published
Phonon effect on single electron transport in two-dot semiconductor devices	A. Valentin, S. Galdin-Retailleau, P. Dollfus	UPS	2	J. Appl. Phys. 106 (2009) 044501	published
Controllable spin-dependent transport in armchair graphene nanoribbon structures	V. Hung Nguyen, V. Nam Do, A. Bournel, V. Lien Nguyen, P. Dollfus	UPS	2	J. Appl. Phys. 106 (2009) 053710	published
Wigner-Boltzmann Monte Carlo approach to nanodevice simulation: from quantum to semiclassical transport	D. Querlioz, H. Nha Nguyen, J. Saint-Martin, A. Bournel, S. Galdin-Retailleau, P. Dollfus	UPS	4	J. Comput. Electron. 8 (2009) 324-335	published
Resonant tunneling and negative transconductance in single barrier bilayer graphene structure	V. Hung Nguyen, A. Bournel, V. Lien Nguyen, P. Dollfus	UPS	2	Appl. Phys. Lett. 95 (2009) 232115	published
Integration of Gd silicate / TiN gate stacks into SOI n-MOSFETs	M. Schmidt, H.D.B. Gottlob, A. Stefani, and H. Kurz	AMO	1	Microelectron., Eng. 86(7-9), pp. 1683-1685, 2009	published
Measurement of effective electron mass in biaxial tensile strained silicon on insulator	S. F. Feste, Th. Schäpers, D. Buca, Q.T. Zhao, J. Knoch, M. Bouhassoune, A. Schindlmayr, S. Mantl	FZJ	1	Applied Physics Letter 95, 182101 (2009)	published
Silicon Nanowire FETs with Uniaxial Tensile Strain	Feste, S.F.; Knoch, J.; Habicht, S.; Buca, D.; Zhao, Q.T.; S. Mantl	FZJ	1	Solid-State Electronics 53, 1257 (2009)	published
Modeling and validation of piezoresistive coefficients in Si hole inversion layers	A. T. Pham, C. Jungemann, B. Meinerzhagen	TUBS	4	Solid-State Electronics, Vol. 53, pp. 1325-1333, 2009	published
MBE Growth of Ge Quantum Dot Structures in Oxide Windows	A. Karmous, O. Kirfel, M. Oehme, E. Kasper, and J. Schulze	USTUTT	2.4	IOP Conf. Series: Materials Science and Engineering 6 (2009) 012020	published
Silicon oxynitride layers fabricated by Plasma Enhanced Chemical Vapor Deposition for CMOS devices	R. Mroczynski, R.B. Beck	WUT	1	ECS Transactions, 25(8), 2009	published
High frequency and noise model of gate-all-around metal-oxide-semiconductor field-effect transistors	B. Nae, B. A. Lazaro, B. Iñiguez	URV	2,4	Journal of Applied Physics Volume: 105 Issue: 7 Article Number: 074505 2009	published
High-frequency compact analytical noise model for double-gate metal-oxide-semiconductor field-effect transistor	A. Lázaro, A. Cerdeira, B. Nae, M. Estrada, B. Iñiguez	URV	4	Journal of Applied Physics, Vol. 105, Issue: 3 Article Number: 034510, 2009	published

Hole Mobility in Ultrathin Double-Gate SOI Devices: The Effect of Acoustic Phonon Confinement	L.Donetti, F.Gamiz, N.Rodriguez and A.Godoy	UGR	4	IEEE Electron Devices Letters, 30 (12), 1338 (2009)	published
Equivalent Oxide Thickness of Trigate SOI MOSFETs With High-k Insulators	F.Ruiz, I.Tienda-Luna, A.Godoy, L.Donetti, and F.Gamiz	UGR	4	IEEE Transactions on Electron Devices, 56 (11), 2711 (2009)	published
Simulation of hole mobility in two-dimensional systems	L.Donetti, F.Gamiz, N.Rodriguez	UGR	4	Semiconductor Science and Technology, 24 (2009) 035016 (7pp)	published
Multiparameter admittance spectroscopy for metal-oxide-semiconductor systems	J.Piscator, B. Raeissi, O.Engström	Chalmers	1	<i>J. Appl. Phys.</i> , 106 ,054510 (2009)	published
The conductance method in a bottom-up approach applied on hafnium oxide/silicon interfaces	J.Piscator, B. Raeissi, O.Engström	Chalmers	1	<i>Appl. Phys. Lett.</i> , 94 , 213507 (2009)	published
A nonparabolicity model compared to tight-binding: The case of square silicon quantum wires	A. Esposito, M. Luisier, M. Frey, and A. Schenk	ETHZ	4	Solid-State Electronics 53 (3), 376 - 382, 2009	published
Quantum transport including nonparabolicity and phonon scattering: application to silicon nanowires	A. Esposito, M. Frey, and A. Schenk	ETHZ	4	Journal of Computational Electronics 8 (3), 336-348 (2009), SpringerLink: 10.1007/s10825-009-0276-0	published
Suppression of gate-induced drain leakage by optimization of junction profiles in 22 nm and 32 nm SOI nFETs	A. Schenk	ETHZ	4	Solid-State Electronics, doi:10.1016/j.sse.2009.12.005	in press DOI
Estimate of Dielectric Density using Spectroscopic Ellipsometry.	W. Davey, O. Bui, I.Z. Mitrovic, M. Werner, S. Hall, P. Chalker	Livuni	1	Microelectronic Engineering, vol. 86, issues 7-9, pp. 1905-1907 (2009)	published
Rare earth silicate formation – a route towards high-k for the 22 nm node and beyond	I.Z. Mitrovic, S. Hall	Livuni	1	Journal of Telecommunications and Information Technology, no. 4, 2009	in print
Defect identification in strained Si/SiGe heterolayers for device applications	E Escobedo-Cousin, SH Olsen, AG O'Neill and H Coulson	UNEW	1&4	Journal of Physics D, vol. 42, pp. 175306	published
The impact of self-heating and SiGe strain-relaxed buffer thickness on the analog performance of strained Si nMOSFETs	OM Alatise, KSK Kwa, S Olsen, and AG O'Neill	UNEW	1&4	Solid State Electronics	in press, DOI
Influence of electron charge states in nanoelectronic building blocks	J. Piscator	Chalmers	1	<i>PhD Thesis, Chalmers, ISBN 978-91-7385-281-4, (2009)</i>	published
Realization of vertical silicon nanowire networks with an ultra high density by top-down approach	X.L. Han, G. Larrieu, E. Dubois	ISEN-IEMN	2	Journal of Nanoscience and Nanotechnology	accepted

Formation of steep, low Schottky-barrier contacts by dopant segregation during nickel silicidation	Feste, S.F.; Knoch, J.; Buca, D.; Zhao, Q.T.; Breuer, U.; and S. Mantl	FZJ	1	Journal of Applied Physics	accepted
Systematic Study of Schottky Barrier MOSFETs with Dopant Segregation on Thin-Body SOI	C. Urban, C. Sandow, Q.-T. Zhao, J. Knoch, S. Lenk, S. Mantl	FZJ	1	Solid-State Electronics	accepted
Ultra thin Ni-silicides with low contact resistance on strained and unstrained silicon	L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, B. Ghyselen, S. Mantl	FZJ	1	IEEE Electron Device Letters	accepted
Nanowire transistors without junctions	J.-P. Colinge, C.-W. Lee, A. Afzalian, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, R. Murphy	Tyndall	2	Nature Nanotechnology	accepted
Compact capacitance modeling of a 3-terminal FET at zero drain-source voltage	B. Iñiguez, O. Moldovan	URV	4	Solid-State Electronics	accepted
Statistical-variability compact-modeling strategies for BSIM4 and PSP	B. Cheng, D. Dideban, N. Moezi, C. Millar, G. Roy, X. Wang, S. Roy, A. Asenov	UoG	4	IEEE Design & Test of Computers	accepted
Improved analog performance in strained Si MOSFETs using the thickness of the silicon germanium strain relaxed buffer as a design parameter	OM Alatise, KSK Kwa, SH Olsen, and AG O'Neill	UNEW	1	IEEE Transactions on Electron Devices	accepted
Reverse graded SiGe/Ge/Si buffers for highcomposition virtual substrates	V.A. Shah, A. Dobbie, M. Myronov, D.R. Leadley	Warwick	1	Journal of Applied Physics	submitted
A Compact Mobility Model for Bulk, Ultra-Thin Body SOI and Double-Gate n-MOSFETs with Different Surface and Channel Orientations. Part I: Fundamental Principles	L. Silvestri, S. Reggiani, E. Gnani, A. Gnudi, G. Baccarani	IUNET-Bo	4	IEEE Trans. on Electron Devices	submitted
A Compact Mobility Model for Bulk, Ultra-Thin Body SOI and Double-Gate n-MOSFETs with Different Surface and Channel Orientations. Part II: Ultra-Thin Silicon Films	L. Silvestri, S. Reggiani, E. Gnani, A. Gnudi, G. Baccarani	IUNET-Bo	4	IEEE Trans. on Electron Devices	submitted
Determination of Strain Tensors in Layer Systems by Precision Ion Channeling Measurements	H. Trinkaus, B. Holländer, D. Buca, R.A. Minamisawa, S. Mantl, JM. Hartmann	FZJ	1	Journal of Applied Physics	submitted
High-frequency compact analytical noise model of gate-all-around MOSFETs	A. Lázaro, B. Nae, M. Cheraflathan, B. Iñiguez	URV	2,4	Semiconductor Science & Technology	submitted

Analytical Modeling of the Gate Tunneling Leakage for the Determination of Adequate High-k Dielectrics in Double-Gate SOI MOSFETs at the 22 nm node	G. Darbandy, R. Ritzenthaler, F. Lime, I. Garduño, M. Estrada, A. Cerdeira and B. Iñiguez.	URV	1,4	Solid-State Electronics	submitted
Multiparameter admittance spectroscopy as a diagnostic tool for interface states at oxide/semiconductor interfaces	B. Raeissi, J. Piscator and O. Engström	Chalmers	1	IEEE Trans. El. Dev.	submitted
The role of mobile charge in oxygen plasma enhanced silicon-to-silicon wafer bonding	B. Raeissi, A. Sanz-Velasco, O. Engström	Chalmers	1	J. Electrochem. Soc.	submitted
Additive Performance Boosters and Sensitivity to Parameter Fluctuations of Silicon Tunnel FETs	K. Boucart, W. Riess, A. M. Ionescu	EPFL	2	IEEE Transactions on Electron Devices	submitted
Asymmetrically strained all-silicon multi-gate n-Tunnel FETs	M. Najmzadeh, K. Boucart, W. Riess, A. M. Ionescu	EPFL	2	Solid-State Electronics, 2010.	submitted

Presentation at the Conferences and Workshops (emphasize if invited lectures)

Title	Author(s)	Nanosil partners	Conference/ Workshop (title)	WP	Date & Location	Type of presentation (oral/poster/invited)	Status (done/accepted/submitted)
Electrical Transport characterization of nano CMOS devices with ultra-thin silicon film	G. Ghibaudo et al.	INPG/FMNT, CEA/LETI, ST, IMEC	9th International Workshop on Junction Technology (IWJT 2009)	4	11-12 June 2009, Kyoto, Japan	Invited keynote paper	Done
SOI as a platform for transition from micro to nano	F. Balestra	INPG-FMNT	ECS Int. Symp. SOI Technology & Devices,	1,2,4	May 2009, San Francisco USA	Invited	Done
Silicon-based devices and materials for nanoscale CMOS and beyond-CMOS	F. Balestra	INPG-FMNT	FTM'2009	1,2,4	June 2009, Sardinia	Invited	Done
SOI- a platform for transition from micro to nano	F. Balestra	INPG-FMNT	IEEE International Semiconductor Conference-CAS	1,2,4	Oct.2009, Sinaia, Romania	Invited	Done
Multi-gate Devices for High Performance, Ultra Low Power and Memory applications	F. Balestra	INPG-FMNT	ECS Int. Symposium "ULSI Process Integration"	1,2,4	Vienna, Austria, Oct. 2009	Invited	Done
3D quantum transport simulations of Si Nanowires: impact of elastic and inelastic scattering	M.G. Pala	FMNT/INPG	SINANO-NANOSIL Workshop	2,4	18 September 2009, Athens (Greece)	Invited	Done
Ultra compact FDSOI transistors including strain and orientation : processing and performance	C. Fenouillet-Beranger, L. Pham Nguyen, P. Perreau, S. Denorme, F. Andrieu, O. Faynot, L. Tosti, L. Brevard, C. Buj, O. Weber, C. Gallon, V. Fiori, F. Boeuf, S. Cristoloveanu, T. Skotnicki	FMNT/INPG, CEA-LETI	14th Int. Symposium on Silicon on Insulator Technology and Devices, 215th Meeting of the Electrochemical Soc.,	4	San Francisco, USA (25-29 mai 2009)	INVITED paper	Done

Floating-body SOI memory: concepts, physics and challenges	M. Bawedin, S. Cristoloveanu, D. Flandre, F. Udrea	INPG/FM NT, UCL	14th Int. Symposium on Silicon on Insulator Technology and Devices, 215th ECS Meeting	4	San Francisco, USA (25–29 mai 2009)	INVITED paper	Done
Cooltronics – a new silicon technology	D.R. Leadley, M. Prest, T.E. Whall, EHC. Parker, M. Meschke, J. Muhonen, J.P. Pekola, J. Ahopelto and M Prunnila	Warwick	9th Symposium Diagnostics and Yield: Advanced silicon devices for the ULSI era	1	Warsaw (2009)	Oral Invited	Done
Accurate effective mobility extraction in SOI MOS transistors	S.M. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, R.J.P Lander, G. Vellianitis, J.R. Watling,	Warwick	9th Symposium Diagnostics and Yield: Advanced silicon devices for the ULSI era,	1	Warsaw (2009).	Oral Invited	Done
Realization of globally strained Ge layers	M. Myronov and D.R. Leadley	Warwick	E-MRS 2009	1	Strasbourg, France, June 8-12, (2009) oral	Oral Invited	Done
Schottky-Barrier Source/Drain MOSFET technology	P.-E. Hellström, M. Östling, V Gudmundsson, J. Luo, Z. Zhang, B. G. Malm and S.-L. Zhang	KTH	Design and Yield 2009	WP 1	22-24 June, Warszawa	Oral/ Invited	Done
Implementation of Schottky Barrier contact technology in ultra scaled MOSFETs	V. Gudmundsson, M Östling, P.-E. Hellström, J. Luo, Z. Zhang, Z. Qiu, B. G. Malm and S.-L. Zhang	KTH	1st Int. Workshop on Si based nano-electronics and –photonics SiNEP-09	WP 1	20- 23rd September 2009	Oral/ Invited	Done
“Perspectives of graphene nanoelectronics: probing technological options with modeling”	G. Iannaccone, G. Fiori, M. Macucci, P. Michetti, M. Cheli, A. Betti, P. Marconcini	IUNET	International Electron Device Meeting	2	2009 Baltimore	Invited	Done
Opportunities and limitations of SOI technology: for RF applications	J.-P. Raskin	UCL	8 th Diagnostics & Yield Symposium	1, 2, 4	June 22-24, 2009, Warsaw, Poland	invited	Done
Assessment of advanced SOI technologies for high-temperature applications	J. Alvarado, V. Kilchytska, D; Flandre	UCL	8 th Diagnostics & Yield Symposium	4	June 22-24, 2009, Warsaw, Poland	invited	Done
SOI technology: an opportunity for RF designers?	J.-P. Raskin	UCL	EUROSIL – 2009, Fifth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits	1, 2, 4	January 19-21, 2009, Göteborg, Sweden	invited	Done
Metallic Source/Drain Architecture for Advanced MOS Technology: an overview	E. Dubois, G. Larrieu, N. Breil, R. Valentin, F. Danneville, D. Yarekha, N. Reckinger, X. Tang, A. Halimaoui, R. Rengel, E. Pascual, A. Pouydebasque, X. Wallart, S. Godey, J. Ratajczak, A. Laszcz, J. Katcki, J.P. Raskin, G. Dambrine, A. Cros, T. Skotnicki	ISEN-IEMN UCL ST ITE USAL	8th Symposium Diagnostics & Yield Advanced Silicon Devices and Technologies for ULSI Era	1	June 22-24, 2009, Warszawa, Poland	Oral Invited	Done

Metallic source/drain for advanced MOS architectures: from material engineering to device integration	E. Dubois, G. Larrieu, N. Breil, R. Valentin, F. Danneville, D. Yarekha, N. Reckinger, X. Tang, A. Halimaoui, R. Rengel, E. Pascual, A. Pouydebasque, X. Wallart, S. Godey, J. Ratajczak, A. Laszcz, J. Katcki, J.P. Raskin, G. Dambrine, A. Cros, T. Skotnicki	ISEN-IEMN UCL ST ITE USAL	SINANO-NANOSIL Workshop Silicon-based CMOS and Beyond-CMOS Nanodevices	1	September 18, 2009, Athens	Oral Invited	Done
Novel channel and dielectric materials for nanoelectronics	S.F. Feste, D. Buca, R.A. Minimisawa, Q.T. Zhao, J.M. Lopes, J. Schubert, B. Holländer, S. Mantl	FZJ	International Workshop on Si based nanoelectronics and photonics	WP 1	Vigo, Spain 20 - 23 September 2009	Invited	Done
Porous Si as a local substrate technology platform for on-chip electronic and sensor applications	A. G. Nassiopoulou	NCSR	TUAT/TEL International Workshop "Innovations of the Silicon, by the Silicon, for the Silicon"	2.4	18-9-2009 Tokyo	Invited	Done
"Ordered arrays of SiO ₂ nanodots with embedded Si nanocrystals: Fabrication and characterization"	A. G. Nassiopoulou	NCSR	216th ECS Meeting – Vienna, Austria, E1 – Analytical Techniques for Semiconductor Materials and Process Characterization	2.4	6-10-2009	Invited	Done
"Silicon nanostructuring through self-assembled masking layers"	Nassiopoulou	NCSR	EMRS 2009_ Symposium M, Strasbourg,	2.4	9-13 June 2009	Invited	Done
Advances in SOI Compact Modeling	B. Iñiguez, R. Ritzenthaler	URV	MOS-AK Workshop	4	Dec. 9 2009, Baltimore (MA, USA)	Invited	Done
CMOS: Is this the end of the beginning or the end of the end?	O. Engström	Chalmers	Nordic Semiconductor Meeting,	1	June 15 - 17, 2009 Reykiavik	Invited	Done
Charging phenomena at the interface between high-k dielectrics and SiO _x interlayers	O. Engström, B. Raeissi, J. Piscator, I.Z.Mitrovic, S. Hall, H.D.B.Gottlob, M. Schmidt, P. Hurley, K. Cherkaoui,	Chalmers, Liverpool, AMO, Tyndall	8th Symposium Diagnostics & Yield Advanced Silicon Devices and Technologies for the ULSI Era	1	June 22 - 24, 2009 Warsaw	Invited	Done
Limitations in future high-k materials	O. Engström	Chalmers	NANOSIL Workshop at ESSDERC	1	Athens, Sept. 14 - 18, 2009	Invited	Done
Classification of energy levels in quantum dot structures by means of depletion layer spectroscopy methods.	M.Kaniewska, O. Engström, M. Kaczmarczyk	ITE, Chalmers	13th International Conference on Defects-Recognition, Imaging and Physics in Semiconductors	2	Wheeling, West Virginia, USA, September 13-17, 2009	Invited	Done
Sub-kT/q subthreshold slope transistors	A.M. Ionescu	EPFL	ESSDERC 2009	2	Athens, Sept. 14, 2009	Invited Tutorial	Done
Simulation of gate leakage currents in UTB MOSFETs and Nanowires	A. Schenk	ETHZ	SINANO-NANOSIL Workshop "Silicon-based CMOS and Beyond-CMOS Nanodevices	4	Athens, September 18, 2009	Invited talk	Done

Simulation of band-to-band tunneling in Si nanoscale devices: The role of junction profiles	A. Schenk	ETHZ	NODE Device Workshop	4	IBM Rüschiikon, Zürich, June 11, 2009	Invited	Done
Rare earth silicate formation – a route towards high-k for the 22 nm node and beyond	I.Z. Mitrovic, S. Hall	Livuni	Diagnostics&Yield 2009	1	Warsaw, Poland, June 2009	invited	Done
Charging phenomena at the interface between high-k dielectrics and SiOx interlayers	O. Engstrom, B. Raeissi, J. Piscator, I.Z. Mitrovic, S. Hall, H.D.B. Gottlob, M. Schmidt, P.K. Hurley, K. Cherkaoui	High-K HGang	Diagnostics&Yield 2009	1	Warsaw, Poland, June 2009	invited	Done
Variability in Nanoscale CMOS and Nanowires	A. Asenov	UoG	NANOSIL Workshop at ESSDERC	4	Sept 09 Athens	Invited	Done
Statistical variability and compact model strategies	A. Asenov	UoG	ECS Meeting	4	Sept 09 Vienna	Invited	Done
Statistical variability: a roadblock for future scaling	A. Asenov	UoG	INSIGHT	4	April 09 Napa	Invited	Done
Static and Low Frequency Noise Characterization of FinFET Devices	K. Bennamane, T. Boutchacha, G. Ghibaudo, M. Mouis, N. Collaert	INPG/FM NT, IMEC	Ultimate Integration on Silicon Conference (ULIS'2009)	4	March 18-20, 2009, Aachen (DE)	Oral	Done
Full-3D real-space treatment of surface roughness in double gate MOSFETs	C. Buran, M. G. Pala, S. Poli, M. Mouis	INPG/FM NT, IUNET	Ultimate Integration on Silicon Conference (ULIS'2009)	2	March 18-20, 2009, Aachen	Oral	Done
Full-3D real-space simulation of surface-roughness effects in double gate MOSFETs	C. Buran, M.G. Pala, S. Poli and M. Mouis	INPG/FM NT, IUNET	13th International Workshop on Computational Electronics (IWCE'2009)	4	May 27-29, 2009, Beijing (China)	Oral	Done
Full-3D Real-Space Simulation of Surface-Roughness Effects in Double-Gate MOSFETs	C. Buran, M.G. Pala, M. Mouis, S. Poli	FMNT-INPG, IUNET	IWCE 2009,	4	27-29 May 2009 Page(s):1 - 4		Done
Special effects in triple gate MOSFETs fabricated on silicon-on-insulator (SOI)	Y. Bae, K-I. Na, S. Cristoloveanu, W. Xiong, C.R. Cleavelin, J.-H. Lee	INPG/FM NT	2009 International Semiconductor Conference (CAS 2009), Volume 1, Page(s):51 - 56	1, 4	October 12-14, 2009, Sinaia (Romania)	Oral	Done
Backscattering coefficient in gate-all-around 3C-SiC nanowire FETs	K. Rogdakis, S. Poli, E. Bano, K. Zekentes, M.G. Pala	FMNT/INPG, IUNET	IEEE NANO 2009	2	26-30 July 2009, Genoa (Italy)	Oral	Done
Low-temperature measurements on Germanium-on-Insulator pMOSFETs: evaluation of the background doping level and modeling of the threshold voltage dependence	W. Van Den Daele, E. Augendre, K. Romanjek, C. Le Roeyr, L. Clavelier, J-F. Damlencourt, E. Guiot, B. Ghyselen, S. Cristoloveanu	INRG/FM NT, CEA-LETI	14th Int. Symposium on Silicon on Insulator Technology and Devices, 215th ECS Meeting	4	San Francisco, USA (25-29 mai 2009)	Oral	Done
Scalability of MSD memory effect.	A. Hubert, S. Cristoloveanu, M. Bawedin, T. Ernst	INPG/FM NT, CEA-LETI	10th Int. Conference on Ultimate Integration of Silicon (ULIS'09)	4	Aachen, Germany, (18-20 mars 2009)	Oral	Done

Study of Si Nanowires Growth by CVD-VLS and Physical Properties	T. Baron, F. Dhalluin, S. Bassem, B. Salhi, H. Abed, A. Potie, M. Panabière, S. Decossas, M. Kogelschatz, L. Montès, F. Oehler, P. Gentile, N. Pauc, M. Den Hertog, J. Rouvière, P. Noe and P. Ferret	INPG, LETI	216th ECS Meeting	4	October 4 - October 9, 2009, Vienna, Austria	Oral	Done
Electrical Characterization of Silicon Nanowires FET	B. Salem, H. Abed, F. Dhalluin, M. Panabière, T. Baron, P. Noe, F. Oehler, N. Pauc and P. Gentile	INPG, LETI	216th ECS Meeting	4	October 4 - October 9, 2009, Vienna, Austria	Oral	Done
Reverse graded virtual substrates for strained Ge devices	D. R. Leadley, V.A. Shah, A. Dobbie and M. Myronov	Warwick	UK Semiconductors 2009	1	July 1-2, 2009, Sheffield, UK	Oral	Done
Characterisation of Strained Ge Epitaxial Layers Grown by RPCVD on Reverse Graded $\text{Si}_{0.2}\text{Ge}_{0.8}$ Relaxed Buffers	V.H. Nguyen, A. Dobbiew, M. Myronov, V.A. Shah, X-C. Liu and D.R. Leadley	Warwick	Institute of Physics Condensed Matter and Materials Physics Conference	1	Warwick, Dec 17-19 (2009).	Poster	Done
TEM analysis of Ge-on-Si MOSFET structures with HfO_2 dielectric for high performance PMOS device technology	DJ Norris, T Walther, AG Cullis, M Myronov, A Dobbie, T Whall, EHC Parker, DR Leadley, B De Jaeger, W Lee, M Meuris, J Watling and A Asenov	Warwick, IMEC, Glasgow	Microscopy of Semiconducting Materials 16 (2009) [Journal of Physics: Conference Series]	1, 4	Oxford, UK, March 2009	Poster	Done
Epitaxial growth of compressive strained Ge layers on reverse linearly graded virtual substrate by RP-CVD	M. Myronov, A. Dobbie, V.A. Shah and D.R. Leadley	Warwick	E-MRS 2009,	1	Strasbourg, France, June 8-12, (2009)	Oral	Done
Effect of $\text{Si}_{1-x}\text{Ge}_x$ Growth Rate on the Threading Dislocation Density in Fully Relaxed $\text{Si}_{1-x}\text{Ge}_x/\text{Si}(100)$ Virtual Substrates Grown at High Temperature by RP-CVD	A. Dobbie, M. Myronov, X. Liu, E. H. C. Parker and D. R. Leadley	Warwick	E-MRS 2009,	1	Strasbourg, France, June 8-12, (2009)	Poster	Done
Low temperature epitaxial growth of compressive strained Ge layers on reverse linearly graded virtual substrate by RP-CVD	M. Myronov, A. Dobbie, V.A. Shah and D.R. Leadley	Warwick	ICSI-6: 6th Int. Conf. Silicon Epitaxy and Heterostructures	1	Los Angeles, California, USA, May 17 - 22, (2009)	Oral	Done
Accurate effective mobility extraction in SOI MOS transistors	S.M. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, R.J.P Lander, G. Vellianitis, J.R. Watling	Warwick	ULIS 2009	1	Aachen, Germany (2009)	Poster	Done
Si/SiO ₂ Quantum Well Solar Cells Based on Lateral Charge Carrier Transport	B. Berghoff, S. Suckow, R. Röfver, B. Spangenberg, H. Kurz	RWTH	24th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC)	WP 2	Hamburg, 21-24.09. 2009	poster	Done
Comparison of measurement and simulation of charge transport in selective energy contacts based on Si quantum dots	S. Suckow, B. Berghoff, B. Spangenberg, H. Kurz	RWTH	24th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC)	2	Hamburg, 21-24.09. 2009	poster	done

Quantum wells based on Si/SiO _x stacks for nano-structured absorbers	B. Berghoff, S. Suckow, R. Röfver, B. Spangenberg, H. Kurz, A. Sologubenko J. Mayer	RWTH	E-MRS Spring Meeting, Symposium B: Inorganic and Nanostructured Photovoltaics	2	Strasbourg, June 8-12, 2009.	Oral	done
Geometric broadening in resonant tunneling through Si quantum dots	S. Suckow, B. Berghoff, B. Spangenberg, H. Kurz	RWTH	E-MRS Spring Meeting Symposium B: Inorganic and Nanostructured Photovoltaics	2	Strasbourg, June 8-12, 2009.	Oral	done
Characterization of dopant segregated Schottky barrier source/drain contacts	V. Gudmundsson, P.-E. Hellström, S.-L. Zhang and M. Östling	KTH	ULIS2009	1	19-20 March, Aachen	Oral	done
"Performance analysis of graphene bilayer transistors through tight-binding simulations", pp. 85-88.	G. Fiori, G. Iannaccone	IUNET	13th International Workshop on Computational Electronics	2	2009 Beijing	Oral	done
"Model of 1D Schottky barrier transistor operating far from equilibrium".	P. Michetti, G. Iannaccone	IUNET	IEEE NANO 2009	2	2009 Genoa	Oral	done
"Physical insights on nanoscale FETs based on epitaxial graphene on Si".	M. Cheli, P. Michetti, G. Iannaccone	IUNET	ESSDERC 2009	2	2009 Athens	Oral	done
"Analytical and TCAD-supported Approach to Evaluate Intrinsic Process Variability in Nanoscale MOSFETs".	V. Bonfiglio, G. Iannaccone	IUNET	ESSDERC 2009	4	2009 Athens	Oral	done
"Shot noise analysis in quasi one-dimensional Field Effect Transistors"	A. Betti, G. Fiori, G. Iannaccone	IUNET	20th International Conference on Noise and Fluctuations	2	2009 Pisa	Oral	done
"Comparison of advanced transport models for nanoscale MOSFETs"	P. Palestri, C. Alexander, A. Asenov, G. Bacarani, A. Bournel, M. Braccioli, B. Cheng, P. Dollfus, A. Esposito, D. Esseni, A. Ghetti, C. Fiegna, G. Fiori, V. Aubry-Fortuna, G. Iannaccone, A. Martinez, Majkusiak B., S. Monfray, S. Reggiani, C. Riddet, J. Saint-Martin, E. Sangiorgi, A. Schenk, L. Selmi, L. Silvestri, J. Walczak	IUNET UGLAS IMEP ETHZ STM TUW L2M	10th International Conference on Ultimate Integration of Silicon	4	2009 Aachen	Oral	Done
"Physical insights on graphene nanoribbon mobility through atomistic simulations"	A. Betti, G. Fiori, G. Iannaccone	IUNET	International Electron Device Meeting	2	2009 Baltimore	Oral	Done
Revised analysis of Coulomb scattering limited mobility in biaxially strained silicon MOSFETs	F. Driussi and D.Esseni	IUNET-UD	European Solid State Device Research Conference (ESSDERC)	4	Athens, Sept. 2009	oral	Done

Experimental and physics-based modeling assessment of strain induced mobility enhancement in FinFETs	N. Serra, F. Conzatti, D. Esseni, M. De Michielis, P. Palestri, L. Selmi, S. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, L. Witters, A. Hikavy, M.J. H'ytch, F. Houdellier, E. Snoeck, T.J. Wang, W.C. Lee, G. Vellianitis, M.J.H. van Dal, B. Duriez, G. Doornbos and R.J.P. Lander	IUNET-UD	Electron Device Meeting (IEDM), paper 4.2	4, 1	Dec. 2009	oral	Done
Drain / Substrate Coupling Impact on DIBL of Ultra Thin Body and Box SOI MOSFETs with undoped Channel	S. Burignat, MK. Md Arshad, D. Flandre, V. Kilchytska, F. Andrieux, O.Faynot P. Scheiblin and J.-P. Raskin	UCL, CEA-LETI	ESSDERC 2009 Conference	4	September 14-19, Athènes, Grèce (2009), pp.141-144.	Oral	Done
Substrate effects in sub-32 nm Ultra Thin SOI MOSFETs with Thin Buried Oxide,.	S. Burignat, D. Flandre, V. Kilchytska, F. Andrieux, O.Faynot and J.-P. Raskin	UCL, CEA-LETI	EuroSOI Conference 2009,	4	January 19-21, Göteborg, Sweden (2009)	Oral	done
Transconductance and Mobility Behaviors in UTB SOI MOSFETs with Standard and Thin BOX,	T. Rudenko, S. Burignat, V. Kilchytska, S. Burignat, J.-P. Raskin, F. Andrieu, O. Faynot, A. Nazarov, V. Lysenko, D. Flandre	UCL, CEA-LETI, ISP Kiev	EuroSOI Conference 2009,	4	January 19-21, Göteborg, Sweden (2009)	Oral	Done
Continuous compact model for MuGFETs simulations.	J. Alvarado, V. Kilchytska, D; Flandre, J. Conde, M. Estrada, A. Cerdeira,	UCL	16th International Conf ; on Mixed Design of Integrated Circuits and Systems	4	25-27 June 2009, Lodz, Poland		Done
Self-aligned single-electron memory fabrication based on Si/SiGe/Si heterostructures	X. Tang, F. Ravoux, E. Dubois, E. Kasper, A. Karmous, N. Reckinger, J.-P. Raskin	UCL, IEMN, USTUTT	35th International Conference on Micro & Nano Engineering (MNE),	2	28 Sept. - 1 Oct. 2009 Ghent, Belgium.	poster	Done
TEM characterization of poly-silicon and silicide fin fabrication processes of FinFETs	J. Ratajczak, A. Aszcz, A. Czerwinski, J. Katcki, X. Tang, N. Reckinger, D. Yarecha, G. Larrieu, E. Dubois	UCL, IEMN	Polish National Conference - Nano2009	1	June 22-26, 2009, Warsaw	poster	Done
Issues associated to rare earth silicide integration in ultra thin FD SOI Schottky barrier nMOSFETs	G. Larrieu, D. Yarekha, E. Dubois, N. Breil, N. Reckinger, X. Tang, A. Halimaoui	UCL, IEMN	215th ECS Meeting	1	24-29 may 2009 in San Francisco, USA	oral	Done
UHV Fabrication of the Ytterbium Silicide as Potential low Schottky Barrier S/D Contact Material for n-type MOSFET	D. Yarekha, G. Larrieu, N. Breil, E. Dubois, S. Godey, X. Wallart, C. Soyer, D. Remiens, N. Reckinger, X. Tang, A. Laszcz, J. Ratajczak, A Halimaoui	UCL, IEMN	215th ECS Meeting		24-29 may 2009 in San Francisco, USA	poster	Done
High-Frequency Performance of Dopant-Segregated NiSi S/D SOI SB-MOSFETs	C. Urban, M. Emam, C. Sandow, Q.-T. Zhao, A. Fox, J.-P. Raskin, S. Mantl	UCL, FZJ	ESSDERC 2009 Conference	1, 4	September 14-19, Athènes, Grèce (2009)	oral	Done

Realization of vertical silicon nanowire networks with an ultra high density by top-down approach	X.L. Han, G. Larrieu, E. Dubois	ISEN-IEMN	International Conference on Nanoscience and Technology	2	1-3 Sep 09, Shanghai, China	Oral	Done
Monte Carlo study of ambipolar transport and quantum effects in carbon nanotube transistors	H. Nha Nguyen, S. Retailleau, D. Querlioz, A. Bournel, P. Dollfus	UPS	SISPAD 2009	2	September 9-11, 2009, San Diego, USA	poster	Done
Effects of edge roughness on the spin-dependent transport in armchair graphene nanoribbon structures	V. Hung Nguyen, V. Nam Do, A. Bournel, V. Lien Nguyen, P. Dollfus	UPS	EDISON 16	2	August 20-24, 2009, Montpellier, France	poster	Done
Decoherence due to electron-phonon scattering in semiconductor nanodevices	D. Querlioz, J. Saint-Martin, P. Dollfus	UPS	IWCE 2009	4	May 27-29 2009, Beijing, China	oral	Done
Sequential transport in a two-dot device	A. Valentin, S. Galdin-Retailleau, P. Dollfus	UPS	IWCE 2009	2	May 27-29 2009, Beijing, China	oral	Done
Wigner Monte Carlo simulation of CNTFET: Comparison between semi-classical and quantum transport	H. Nha Nguyen, D. Querlioz, S. Galdin-Retailleau, A. Bournel, P. Dollfus	UPS	IWCE 2009	2	May 27-29 2009, Beijing, China	oral	Done
Effect of access resistance on apparent mobility reduction in nano-MOSFET	K. Huet, J. Saint-Martin, A. Bournel, D. Querlioz, P. Dollfus	UPS	ULIS 2009	4	March 18-20, Aachen, Germany	oral	Done
Impact of strain on p-DGMOS performance using full-band Monte Carlo simulation	V. Aubry-Fortuna, K. Huet, A. Bournel, D. Rideau, C. Chassat, P. Dollfus	UPS	ULIS 2009	4	March 18-20, Aachen, Germany	oral	Done
Mobility measurements in Gd silicate/TiN SOI and sSOI n-MOSFETs	M. Schmidt, H.D.B. Gottlob, D. Buca, S. Mantl and H. Kurz	AMO, FZ-Jülich	International Semiconductor Device Research Symposium (ISDRS 2009)	1	College Park, MD, USA, Dec. 9-11, 2009.	oral	Done
Mobility Extraction of UTB n-MOSFETs down to 0.9 nm SOI thickness	M. Schmidt, M.C. Lemme, H.D.B. Gottlob, H. Kurz, F. Triussi, L. Selmi	AMO, IU.NET	International Conference on Ultimate Integration of Silicon (ULIS 2009)	3, 4	March 18-20, 2009 - Aachen, Germany	oral	Done
Scaling potential and MOSFET integration of thermally stable Gd silicate dielectrics	H.D.B. Gottlob, M. Schmidt, A. Stefani, M.C. Lemme, H. Kurz, I.Z. Mitrovic, W.M. Davey, S. Hall, M. Werner, P.R. Chalker, K. Cherkaoui, P.K. Hurley, J. Piscator, O. Engström, S.B. Newcomb	AMO, LIVUNI, Tyndall-UCC, Chalmer s	Conference of Insulating Films on Semiconductors (INFOS 2009)	1	Cambridge, UK, June 29 - July 01, 2009	oral	Done
Integration of Gd silicate / TiN gate stacks into SOI n-MOSFETs	M. Schmidt, H.D.B. Gottlob, A. Stefani, and H. Kurz	AMO	Conference of Insulating Films on Semiconductors (INFOS 2009)	1	Cambridge, UK, June 29 - July 01, 2009	poster	Done
Platforms for planar & non-planar ultrathin silicon	M. Schmidt, H.D.B. Gottlob, J. Bolten, T. Wahlbrink, T. Mollenhauer, M. Bückins, T.E. Weirich, F. Dorn, J. Mayer, H. Kurz	AMO	EUROSOI 2009	2	Göteborg, Sweden, Jan. 19-21, 2009	oral	Done

Uniaxial strain relaxation in He-implanted (110) oriented SiGe layers	D. Buca, RA. Minamisawa, H. Trinkaus, B. Holländer, V. Destefanis, JM. Hartmann, S. Mantl	FZJ	International Conference on Silicon Epitaxy and Hetero-structures	1	Los Angeles May 17-22, 2009	oral	Done
Performance enhancement of uniaxially-tensile strained Si NW-nFETs fabricated by lateral strain relaxation of SSOI	Feste, S.F.; Knoch, J.; Habicht, S.; Buca, D.; Zhao, Q.T.; S. Mantl	FZJ	ULIS 2009	1	Aachen 18-20 March, 2009	oral	Done
Strained and Unstrained Si Nanowire FETs	S.F. Feste, S. Habicht, Q.T. Zhao, D. Buca, and S. Mantl	FZJ	ESSDERC	1	Athens, Greece 14-18 Sept 2009	Oral	Done
Investigation of Arsenic dopant segregation layers for scaled Schottky-Barrier MOSFETs	Feste, SF; Urban, C; Knoch, J; Zhao, QT; Buca, D; Breuer, U; Mantl S	FZJ	E-MRS Spring Meeting 2009	1	Strasbourg, June 08-12, 2009	Poster	Done
Systematic study of SOI SB-MOSFETs with dopant segregation	C. Urban, Q. T. Zhao, C. Sandow, S. Lenk, S. Mantl	FZJ	EUROSIOI 2009	1	Göteborg, Jan.19. – 21, 2009	Oral	Done
Schottky Barrier Height tuning using Sb Segregation	C. Urban, Q. T. Zhao, C. Sandow, M. Müller, S. Mantl	FZJ	MAM 2009	1	Grenoble, Mar 8. – 9, 2009	Oral	Done
High Performance Schottky Barrier MOSFETs on UTB SOI	C. Urban, C. Sandow, Q.-T. Zhao, S. Mantl	FZJ	ULIS 2009	1	Aachen, March 18-20, 2009	Oral	Done
Ultra thin Ni-silicides with low contact resistance on SOI and strained-SOI	L. Knoll, Q.T. Zhao, S. Habicht, C. Urban, B. Ghyselen, S. Mantl	FZJ	Proc. of Intern. Conf. Solid State Dev. Mat.	1	Sendai, Japan, Oct. 7-9, 2009	Poster	Done
Modeling of piezoresistive coefficients in Si hole inversion layers	A. T. Pham, C. Jungemann, B. Meinerzhagen	TUBS	Proceedings of ULIS, Aachen (Germany), 2009	4		oral	Done
Simulation of mobility variation and drift velocity enhancement due to uniaxial stress combined with biaxial strain in Si PMOS	A. T. Pham, C. Jungemann, B. Meinerzhagen	TUBS	Proceedings of IWCE-13, pp. 45-48, Beijing (China), 2009	1, 4		oral	Done
MBE Growth of Ge Quantum Dot Structures in Oxide Windows	A. Karmous, O. Kirfel, M. Oehme, E. Kasper, and J. Schulze	USTUTT	E-MRS Symposium K: Semiconductor Nanostructures towards Electronic and Optoelectronic Device Applications II	2.4	June 8 - 12, 2009 Congress Center, Strasbourg, France	Oral	Done
Charge pumping characterization of MOSFETs with HfSiON gate dielectric	K. Jasinski, G. Gluszko, L. Lukasiak, A. Jakubowski	WUT	14 th Canadian Semiconductor Technology Conf. Nano and Giga Challenges in Electronics, Photonics and Renewable Energy	1	Aug. 10-14, 2009 Hamilton, Canada	poster	Done
Signal generator for extensive characterization of MOS devices	M. Iwanowicz, Z. Pióro, L. Lukasiak, A. Jakubowski	WUT	14 th Canadian Semiconductor Technology Conf. Nano and Giga Challenges in Electronics, Photonics and Renewable Energy	1	Aug. 10-14, 2009 Hamilton, Canada	poster	Done

Charge pumping characterization of MOSFETs with SiO ₂ /BaTiO ₃ as a gate stack	G. Gluszko, P. Firek, L. Lukasiak, J. Szmidt, A. Jakubowski	WUT	8th Symp. Diagnostics & Yield : Advanced Silicon Devices and Technologies for the ULSI Era	1	June 22-24 2009, Warszawa (Poland)	poster	Done
Silicon oxynitride layers fabricated by Plasma Enhanced Chemical Vapor Deposition for CMOS devices	R. Mroczyński, R.B. Beck	WUT	216th Meeting of Electrochemical Society – EuroCVD-17 and CVD-17	1	October 4-9 2009, Vienna (Austria)	poster	Done
Reliability issues of double gate dielectric stacks based of hafnium dioxide (HfO ₂) layers for non-volatile semiconductor memory (NVSM) applications	R. Mroczyński, R.B. Beck	WUT	8th Symp. Diagnostics & Yield : Advanced Silicon Devices and Technologies for the ULSI Era	1	June 22-24 2009, Warszawa (Poland)	poster	Done
High Frequency and Noise Compact Model of Gate-All-Around MOSFETs Including Quantum Effects	B. Nae, A. Lázaro, B. Iñiguez	URV	EUROSOI Workshop	2,4	January 19-21 2009, Göteborg (Sweden)	Poster	Done
A High Frequency Compact Noise Model for Double-Gate MOSFET Devices	A. Lázaro, A. Cerdeira, B. Nae, M. Estrada, B. Iñiguez	URV	20th International Conference on Noise and Fluctuations	4	June 14-19 2009, Pisa (Italy)	Oral	Done
2D Physics-based Compact Model for Channel Length Modulation in Lightly Doped DG FETs	M. Weidemann, A. Kloes, M. Schwarz, B. Iñiguez	URV	International Conference on Mixed Design of Integrated Circuits (MIXDES)	4	June 25-27, Łódź (Poland)	Oral	Done
2D physics-based compact model of channel length modulation for asymmetrically biased double-gate MOSFETs	M. Weidemann, A. Kloes, M. Schwarz, B. Iñiguez	URV	ESSDERC Fringe	4	Sept. 14-19 2009, Athens (Greece)	Poster	Done
2D analytical solution of potential in lightly doped Schottky barrier double-gate MOSFET	M. Schwarz, M. Weidemann, A.Kloes, B. Iñiguez	URV	ESSDERC Fringe	4	Sept. 14-19 2009, Athens (Greece)	Poster	Done
2D Compact Modeling of the Threshold Voltage in Triple- and Pi-gate Transistors	R. Ritzenthaler, F. Lime, and B. Iñiguez, O. Faynot, S. Cristoloveanu	URV, CEA-LETI, INPG	International Semiconductor Device Research Conference (ISDRS 2009)	4	December 9-11, College Park, MA (USA)	Poster	Done
Analytical Modeling of the Gate Tunneling Leakage for the Determination of Adequate High-K Dielectrics in 22 nm Double-Gate SOI MOSFETs	G. Darbandy, R. Ritzenthaler, F. Lime, I. Garduño, M. Estrada, A. Cerdeira and B. Iñiguez.	URV	International Semiconductor Device Research Conference (ISDRS 2009)	4	December 9-11 2009, College Park, MA (USA)	Oral	Done
Two-Dimensional Model for the Potential Profile in a Short Channel Schottky Barrier DG-FET	M. Schwarz, M. Weidemann, A. Kloes, B. Iñiguez	URV	International Semiconductor Device Research Conference (ISDRS 2009)	4	December 9-11 2009, College Park, MA (USA)	Poster	Done
Analysis and Modeling of the Pinch-Off Point in a Lightly Doped Asymmetrically Biased Double Gate MOSFET	M. Weidemann, A. Kloes, M. Schwarz, B. Iñiguez	URV	International Semiconductor Device Research Conference (ISDRS 2009)	4	Dec. 9-11 2009, College Park, MA (USA)	Poster	Done
High frequency compact noise modelling of Multi-Gate MOSFETs	A. Lázaro, A. Cerdeira, B. Nae, M. Estrada and B. Iñiguez	URV	MOS-AK Workshop	4	April 3 2009, Frankfurt-Oder Germany	Poster	Done

Modeling of the subthreshold characteristics of Triple-Gate Transistors: impact of the channel dimensions and back-gate bias	R. Ritzenthaler, F. Lime and B. Ifiguez	URV	MOS-AK Workshop	4	September 18 2009, Athens (Greece)	Poster	Done
Wafer bonding strength increased by mobile ions.	Raeissi, Bahman; Sanz-Velasco, Anke; Engström, Olof:	Chalmes	EUROSOI 2009	1	Göteborg January 19 -21, 2009	Poster	Done
The influence of orientation and strain on the transport properties of sal Trigate nMOSFETs	I.Tienda-Luna, A.Godoy, F.Ruiz, F.Gamiz	UGR	ESSDERC	4	Athens, Sept 209		Done
Effect of arbitrary orientation and strain on Surrounding Gate Transistors	I.Tienda-Luna, A.Godoy, F.Ruiz, and F.Gamiz	UGR	International Workshop on Computational Electronics,	4	2009 (Beijing, China)		Done
A-RAM: Novel capacitor-less DRAM memory	N.Rodriguez, S.Cristoloveanu, F.Gamiz	UGR, INP, LETI	IEEE Inetrnational SOI COnference	4	San Francisco USA		Done
Quantization Effects in Silicided and Metal Gate MOSFETs	N.Rodriguez, F.Gamiz, R.Clerc, C.Sampedro, A.Godoy, G.Ghibaudo	UGR, INPG	ULIS 2009	4	March 2009 Aachen	oral	Done
Comparison of the electrostatics of bulk and SOI trigate MOSFETs	F.Garcia-Ruiz, A.Godoy, I.Tienda-Luna, F.Gamiz	UGR	Symp. Of Electrochemical Society	4	San Francisco		Done
A model for robust electrostatic design of nanowire ETs with arbitrary polygonal cross sections	Luca de Michielis, Luca Selmi Adrian M. Ionescu	EPFL/ IUNET (Uni Udine)	ESSDERC 2009	1, 2	Athens, Sept. 14, 2009	Oral	Done
Improvement of the Effective Mass Approximation for Silicon Nanowires	A. Esposito, M. Frey, and A. Schenk	ETHZ	Colloque Numérique Suisse	4	University of Basel, April 24, 2009	poster	Done
Boundary Conditions for Incoherent Quantum Transport	M. Frey, A. Esposito, and A. Schenk	ETHZ	International Workshop on Computational Electronics (IWCE-13)	4	Beijing, China, May 27-29, 2009		Done
Impact of Strain on the Performance of high-k/metal replacement gate MOSFETs	X. Wang, S. Roy, and A. Asenov	UoG	Ultimate Integration on Silicon (ULIS 2009)	4	Aachen Germany, March 18-20, 2009		Done
Efficient simulation of 6s VT distribution due to random discrete dopants	D. Reid, C. Millar, G. Roy, S. Roy and A. Asenov	UoG	Ultimate Integration on Silicon (ULIS 2009)	4	Aachen Germany, March 18-20, 2009	Oral	Done
Estimate of Dielectric Density using Spectroscopic Ellipsometry	W. Davey, O. Buiu, I. Mitrovic, M. Werner, S. Hall, P. Chalker	Livuni	INFOS 2009	2	Cambridge UK June 2009	oral	Done
3D analysis of strain in an electrically measured strained SiGe MOSFET	SH Olsen et al	UNEW	Microscopy of Semiconducting Materials (MSM)	1	Oxford, UK, March 2009	oral	Done
A design methodology for maximizing the voltage gain of strained Si MOSFETs using the thickness of the silicon-germanium strain relaxed buffer as a design parameter	OM Alatisse et al	UNEW	ISDRS	1	Washington DC, USA, December 2009	oral	Done

Strain characterization of Si wires	L Sanderson, P Dobrosz, SH Olsen, SJ Bull, S Mantl and D Buca	UNEW, FZJ	International Conference on Metallurgical Coatings and Thin Films (ICMCTF)	1, 2 & 4	San Diego, USA, April 2009	oral	Done
Investigation of oxidation-induced strain in a top-down Si nanowire platform	M Najmzadeh, D Bouvet, A Ionescu, P Dobrosz and SH Olsen	UNEW, EPFL	INFOS	1, 2, 4	Cambridge, UK 2009	oral	Done
Silicon nanowires with lateral uniaxial tensile stress profiles for high electron mobility gate-all-around MOSFETs	M Najmzadeh, L De Michielis, D Bouvet, P Dobrosz, SH Olsen and A Ionescu	UNEW, EPFL	Micro- Nano Engineering	1, 2, 4	Ghent, Belgium 2009	oral	Done
Capturing intrinsic parameter fluctuations using the PSP compact model	B. Cheng, D. Dideban, N. Moezi, C. Millar, G. Roy, X. Wang, S.Roy, A. Asenov	UoG	DATE 2010	4			accepted
Analytical Modeling of direct tunneling Current through SiO ₂ /high-k Gate Stacks for the Determination of Suitable High-k Dielectrics for Nanoscale Double-Gate MOSFETs	G. Darbandy, R. Ritzenthaler, F. Lime, S. I. Garduño, M. Estrada, A. Cerdeira, and B. Iñiguez	URV	EUROSOI Workshop	1, 4	January 25-27 2010, Grenoble (France)	poster	accepted
An analytical compact model for Schottky-Barrier Double Gate MOSFETs	M. Balaguer, B. Iñiguez, J. B. Roldán	URV, UGR	EUROSOI Workshop	1,4	January 25-27 2010, Grenoble	poster	accepted
A 2D analytical model of threshold voltage for Pi-gate FinFET transistors	R. Ritzenthaler, M. Tang, O. Faynot, F. Lime, F. Prégaldiny, C. Lallement, S. Cristoloveanu, and B. Iñiguez	URV, CEA-LETI, INPG	EUROSOI Workshop	4	January 25-27 2010, Grenoble (France)	oral	accepted
Substrate bias effects in MuGFETs	C.W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. Dehdashti-Akhavan, P. Razavi, J.P. Colinge	Tyndall, INPG, UCL	EUROSOI 2010	2	Grenoble, Jan 2010	Poster	accepted
3D Simulation of RTS Amplitude in Accumulation-Mode and Inversion-Mode Trigate SOI MOSFETs	Ran Yan, Ailbhe Cullen, Aryan Afzalian, Isabelle Ferain, Chi-Woo Lee, Nima Dehdashti, Pedram Razavi and J.P. Colinge	Tyndall, UCL	EUROSOI 2010	2	Grenoble, Jan 2010	Poster	accepted
Comparison of Breakdown Voltage in Bulk and SOI FinFETs	P. Razavi, R. Duane, R. Yan, I. Ferain, N. Dehdashti-Akhavan, R. Yu, C.W. Lee, J.P. Colinge	Tyndall	EUROSOI 2010	2	Grenoble, Jan 2010	Oral	accepted
Backgate bias and stress level impact on Giant Piezoresistance effect in thin silicon films and nanowires	V. Passi, F. Ravaux, E. Dubois, J.-P. Raskin	UCL IEMN	IEEE MEMS	2	23-28 January 2010 Hongkong	Poster	accepted
Gate-edge charges related effects and performance degradation in advanced multiple-gate MOSFETs	V. Kilchytska, J. Alvarado, N. Collaert, R. Rooyackers, S. Put, C. Claeys, D. Flandre	UCL, IMEC	EuroSOI 2010	4	January 2010, Grenoble	Oral	accepted