

PhD Studentship at Université catholique du Levant

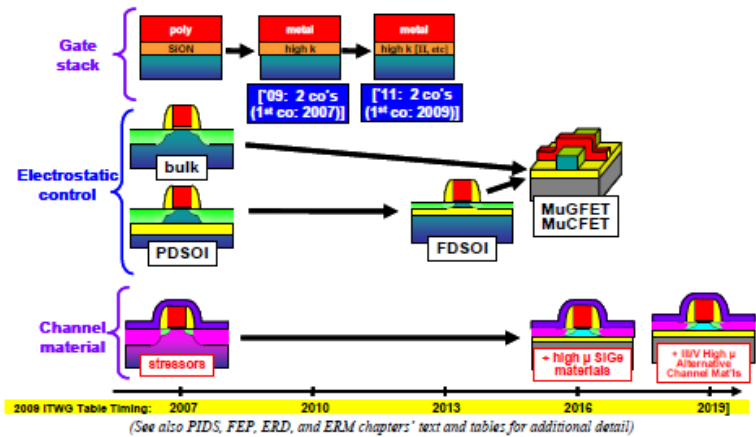
Towards highly-efficient 10nm MOSFETs

Duration: 3 years. 2011- 2014

This research project is funded by FNRS (Fond National de la Recherche Scientifique belge) and will be performed in a close collaboration with other European research projects (Nanosil, Nanofunction, etc.) on related subjects.

Introduction

With the transition towards 10 nm gate length, new materials will be incorporated along with non-classical architectures. Device length shrinkage implies simultaneous reduction of other device dimensions as film thickness (which in turn degrades series resistance and demand for Schottky barrier (SBC) contacts) and gate oxide thickness (which calls for new high-k oxides), in order to improve gate control over the channel first in ultra-thin body (UTB) planar MOSFETs, then in double and triple-gate FETs and finally in quadruple-gate-around FETs or nanowires (NW).



2009 ITRS "Equivalent Scaling" Process Technologies Timing"; PIDS/FEP – Simplified Transistor Roadmap, Original Source: ITRS (Exec. Summary, Fig. 8c), European Nanoelectronics Initiative Advisory Council (ENIAC).

Main objective of the proposed project is an in-depth exploration of peculiar physical phenomena arising from both new materials (strained silicon, silicides, high-k, etc.) and device architectures (UTB MOSFETs, multiple-gate (MuG) FETs, Si NW, etc.), related to MOSFET downscaling towards 10 nm. Within the project, different device options will be investigated through electrical measurements and physical device simulations from the point of view of device physical behaviors and performance as well as reliability and variability perspectives.

Characterization will be carried out on different devices processed in the frame of international projects in which we are involved and thanks to bilateral collaborations with other research centers (IMEC, CEA-LETI, Juelich, Tyndall, IEMN ? etc.).

Description of work

The project intends to explore the following open scientific questions.

- Objective and accurate evaluation of transport properties in advanced devices.
- Impact of leakage current on both static and dynamic transistor behaviors resulting from thin (and high-k) gate dielectrics and channel materials with small energy-gap
- Introduction of UTB and UTB² (with thin buried oxide) device architectures calls for in-depth analysis of substrate bias, optimization of both BOX and film thicknesses, substrate doping.
- Reliability tradeoffs associated with new materials /architectural options
- Variability analyses in the extended temperature and frequency ranges

Tasks to be tackled by the candidate will be:

Task 1. TCAD physical device simulations (including extreme conditions as high temperature, radiation, stress) to allow physical insight on the effects that occur in the device and to support experimental results and explain the origin of new phenomena.

Task 2. DC, low- and high-frequency measurements on advanced devices (either UTB / UTB², or MuGFETs, NWs, etc.) with dimensions down to below-32 nm, extraction of equivalent circuits.

Task 3. Wide temperature range and 4-point bending measurements (for inducing traction or compression stress in the device) targeting revealing and understanding of new physical phenomena as well as reliability assessment.

Task 4. Variability assessment particularly focused on effect of extrinsic parameters, development of new assessment techniques, and reliability related issues (i.e. variability related to temperature effect, mechanical stress effect, etc.)

Requirements

The candidate must have obtained a Master degree in electronic engineering, physics, or a related field. Preferably he/she should already have a good background in solid-state physics and be familiar with electrical characterization and TCAD simulations. He/she has to send a CV, a motivation letter, copies of degree certificates, academic record and a letter of recommendation of his/her Master thesis supervisor.

Contacts

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