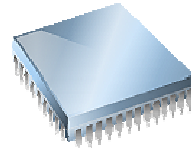
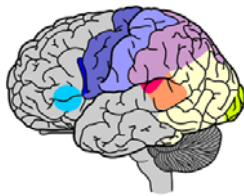


BIECS'09

Athens, Greece
Friday 18th September 2009



Brain-Inspired Electronic Circuits and Systems (BIECS) 2nd International Workshop Held at ESSDERC/ESSCIRC 2009 <http://www.essderc2009.org/>



The workshop will be held following the ESSDERC/ESSCIRC Conferences in Athens, Greece. It is supported by the EU Network of Excellence NANOSIL, Visionary Project 2.5.1. It is also related to the UK Electronics Knowledge Transfer Network, UK which promotes the microelectronics design Grand Challenge: 'Building Brains' which seeks to establish new computing paradigms, inspired by neural activity in the brain.

Significant research has focused on the development of Neural Network (NN) models in Brain-Inspired Electronic Systems that can be implemented in hardware and used to inspire new techniques for real-time computations. However, there exist several fundamental bottlenecks that restrict the progress towards biological scale networks in hardware, such as power consumption, compactness of neuron cells and interconnect, off-chip versus on-chip training. More immediate applications relate to, for example, fault-tolerant or evolutionary computational systems.

To tackle these challenges, innovation is required at all levels of the design hierarchy: novel devices that can exhibit neural functionality with ultra small footprint, schemes to aggregate the devices into appropriate functional building blocks or 'standard neural cells', interconnection schemes that can address the massive parallelism of the brain, and finally electronic systems that can tackle useful problems competitively and at a lower cost than standard approaches.

The objective of the Grand Challenge: 'Building Brains' is to focus efforts in creating microelectronic designs and architectures that deliver very high levels of performance for this area, and thereby help test hypotheses and explore the wider space of asynchronous event-coupled dynamical systems. Progress towards this Grand Challenge would create systems enabling much larger neural models to be simulated than is possible at present. This is likely to be a significant contribution to the higher-level Grand Challenge of understanding the architecture of the brain and mind, whose impact upon humanity would be dramatic.

Workshop Organisation: Liam McDaid, University of Ulster, UK; Jim Harkin, University of Ulster, UK; Steve Hall, University of Liverpool, UK

Researchers interested in this area of research are welcome to attend this event and invited to present posters. Please submit your poster along with a short description (Max. 300 words) in MS Word format to: lj.mcdaid@ulster.ac.uk. Deadline for poster submission is 31st August 2009 (Max. poster size 1.5 metre x 1.5metres).

BIECS' 09
Workshop Programme
Friday 18th September 2009

9:00 Introduction and Overview

9:10 Tadashi Shibata, University of Tokyo: “A VLSI Brain System Mimicking the Processing in the Mind”

9.50 Valeriu Beiu, UAE University: “Connectivity and Scalability Issues for Realisation of Biologically Plausible Nano-electronic Systems”

10:30 **Coffee and Posters** – *Interested delegates are encouraged to contribute a poster to promote their research*

11:10 Steve Furber, University of Manchester: “Biologically-Inspired Massively-Parallel Architectures - computing beyond a million processors”

11:50 Wayne Luk, Imperial College: “Accelerating Neural Models with FPGAs and GPUs”

12:30 Lunch

13:30 Felix Schuermann, EPFL: “The Blue Brain Project - Simulation-based Research in Neuroscience”

14:10 Johannes Schemmel, University of Heidelberg: “The FACETs project”

14:50 Discussion and Coffee
Panel session with speakers

15:30 Final Comments and Close of Workshop

BIECS'09 Abstracts

Tadashi Shibata: A VLSI Brain System Mimicking the Processing in the Mind

The research aiming at building a human-like perception and understanding system best utilizing the state-of-the-art silicon VLSI technology is presented. Rather than building electronic circuits following the physiological reality in biological systems, we are mimicking the processing going on in our mind. Based on the premise that the association to the past experience and the retrieval of the most similar event from the brain memory is the very basis of perception and understanding, we are developing a psychologically-inspired VLSI brain model system. How to implement such ideas in VLSI circuits using both analog and digital CMOS technologies is presented. The algorithms for image representation and its application to robust image perception are also presented and discussed.

Valeriu Beiu: Connectivity and Scalability Issues for Realisation of Biologically Plausible Nanoelectronic Systems

This presentation will set out to address the key limiters of scalability and discuss the means of increasing the numbers of devices on a chip to biologically plausible levels, i.e., investigate biologically inspired connectivity solutions for future nanoelectronic systems. The significance of brain-inspired connectivity comes from the fact that the mammalian brain is one of the most efficient and remarkably robust network of processing elements currently known to mankind. One reason that scalability is so important is that much of the brain's computing power comes from its massive parallelism. The global connectivity of the brain will be analyzed along with the way it communicates locally. We will first of all compare the brain's connectivity (based on neurological data) with well-known computer network topologies (used in super-computers). The comparison will reveal how well brain's connectivity agrees with Rent's rule. However, the known network topologies fall short of being strong contenders for mimicking the brain, therefore emphasis will be placed upon detailed Rent-based (top-down) modeling of two-layer hierarchical networks. This analysis will identify generic network topologies which when combined could mimic brain's connectivity. The range of granularities (i.e., number of gates/cores/neurons) where such mimicking is possible will be presented and discussed. Wire length estimates will follow and will help in the understanding other important parameters like power and reliability. For local interconnects, issues in terms of latency, energy dissipated and signal integrity are inherent problems that normally act to limit the scalability and can negate any computational advantages of parallelism. Various schemes used for reducing the interconnecting density such as Pulsed Wave Interconnect, Address Event Decoding, and Multiple Valued Logic, all have deficiencies which prevent them from scaling towards biologically plausible levels, while Time Multiplexed Architectures seems to exhibit stronger potential. Last but not least, technologies based on standing-waves, solitons, plasmons, and photonics will be evaluated, while models that treat materials' structure atomistically will also be mentioned. These should have implications for the design of future networks-on-chip in general (short term), and for the burgeoning field of multi-/many-core processors in particular (medium term), as well as for forward-looking investigations on emerging brain-inspired (3D) nano-architectures (in the long run).

Steve Furber: Biologically-Inspired Massively-Parallel Architectures - Computing Beyond a Million Processors

The SpiNNaker project aims to develop parallel computer systems with more than a million embedded processors. The goal of the project is to support large-scale simulations of systems of spiking neurons in biological real time, an application that is highly parallel but also places very high loads on the communication infrastructure due to the very high connectivity.

Wayne Luk: Accelerating Neural Models with FPGAs and GPUs

This talk describes recent work on accelerating neural network models with Field-Programmable Gate Arrays (FPGAs) and Graphics Processing Units (GPUs). First, we explain how FPGAs can achieve a compromise between model complexity and simulation speed, such that a fully-connected network of 1024 neurons based on the biologically plausible Izhikevich spiking neuron model can be simulated at 100 times real-time speed. Second, we present a GPU design capable of real-time simulation of around 40000 neurons with 1000 synapses per neuron and a mean firing rate of 10 Hz.

Felix Schuermann: The Blue Brain Project - Simulation-based Research in Neuroscience

Mammalian brains are arguably the most complex structures known to man. In 1mm³ of the neocortex of a rat there are 10,000 nerve cells with close to 1km of fibres and tens of millions of synapses. Unifying experimental biology and high-performance computing, the Blue Brain Project (<http://bluebrain.epfl.ch>) is an undertaking to introduce simulation-based research to neuroscience, i.e. enabling researchers to test hypothesis of function and malfunction "in silico".

Over the last 4 years an interdisciplinary team of 35 researchers has cast the reverse-engineering of the biological pieces and the forward construction of detailed mathematical models in an iterative process that allows continuous refinement. Using the computational power of a 4-rack BlueGene/L, a dedicated framework of software tools has been built that allows a completely data-driven model generation and simulation of a piece of rat brain. In order to put the expert into the loop, extensive use of visualization and interactive analysis is made, which is powered by another dedicated supercomputer in order to realize short turn-around times.

Johannes Schemmel: The FACETS Project

This talk presents the large scale artificial neural network model developed within the European research project "FACETS". The FACETS VLSI model consists of a multitude of interconnected network modules. Each module uses a single 20cm silicon wafer, a method called wafer-scale integration, to implement 40 million plastic synapses. The implementation includes continuous-time analog neurons with up to 16k inputs. These neurons are highly accelerated compared to biological real time. A novel interconnection and routing scheme facilitates the mapping of a multitude of network models derived from biology to the VLSI neural network while maintaining a high resource usage. The FACETS wafer-scale network uses several techniques to reduce power consumption and enhance fault tolerance to a level allowing the integration of whole uncut silicon wafers into the system. Limiting the power consumption of the dense interconnection network providing the necessary communication bandwidth is a critical aspect of system integration. Thus, a novel asynchronous low-voltage signaling scheme is presented that makes the wafer-scale approach feasible by reducing the total power consumption while simultaneously providing a flexible and programmable network topology.

BIECS'09 Speaker Biographies

Professor Tadashi Shibata

Tadashi Shibata is Professor at Department of Electrical Engineering and Information Systems, The University of Tokyo. After working in industry (Toshiba Corporation) as a VLSI device and manufacturing engineer for 12 years, he came back to academia. He proposed the concept of Neuron MOS transistor (multiple-input floating-gate MOS device) in 1991 and developed various new-concept circuits using Neuron MOS. His current research interest is to develop human-like intelligent systems based on the psychologically-inspired VLSI brain model using state-of-the-art silicon technology.

Professor Steve Furber

Steve Furber is the ICL Professor of Computer Engineering in the School of Computer Science at the University of Manchester. He received his B.A. degree in Mathematics in 1974 and his Ph.D. in Aerodynamics in 1980 from the University of Cambridge, England. From 1980 to 1990 he worked in the hardware development group within the R&D department at Acorn Computers Ltd, and was a principal designer of the BBC Microcomputer and the ARM 32-bit RISC microprocessor. Upon moving to the University of Manchester in 1990 he established the Amulet research group which has interests in asynchronous logic design and power-efficient computing, and which merged with the Parallel Architectures and Languages group in 2000 to form the Advanced Processor Technologies group. Steve is a Fellow of the Royal Society, the Royal Academy of Engineering, the British Computer Society, the Institution of Engineering and Technology and the IEEE.

Professor Wayne Luk

Wayne Luk is Professor of Computer Engineering at Imperial College London, and is Visiting Professor at Stanford University. His research interests include theory and practice of accelerator technologies, custom computing, reconfigurable architectures, and design automation.

Professor Valeriu Beiu

Dr. Bieu (S'92-M'95-SM'96) received the MSc in CE from the "Politehnica" University of Bucharest (Romania), in 1980, and the PhD with summa cum laude in EE from the Katholieke Universiteit Leuven (Belgium), in 1994. Upon graduation, for two years he has been working on high-speed CPUs and FPU's with the Research Institute for Computer Techniques (Bucharest, Romania), prior to rejoining the "Politehnica" University of Bucharest. In 1990 he co-founded Spring Software Consult (Bucharest, Romania), and since 1991 has been on leave of absence: Katholieke Universiteit Leuven (1991-1994, Belgium), King's College London (1994-1996, UK), and Los Alamos National Laboratory (1996-1998, USA). In 1998 he co-founded RN2R (Dallas, USA) a VLSI IP startup company, and was its Chief Technical Officer (1998-2001). In 2001 he joined the School of EE&CS, Washington State University (USA). Since 2005 he is a Visiting Professor with the School of Computing & Intelligent Systems, University of Ulster (UK), and since 2006 he is also the Vice Dean for Research and Graduate Studies, College of Information Technology, United Arab Emirates University (UAE). His main research interests are VLSI-efficient designs (i.e., very low-power and highly reliable) and emerging nano-architectures (massively parallel, communication starved, adaptive/reconfigurable, fault-tolerant, and neural inspired), as well as their optimized designs (like cellular and systolic arrays,

artificial neural networks, etc.), being the founder of the Centre for Neural Inspired Nano Architectures (CNINA) as well as co-PI of the Emirates Centre for Nanoscience and Nanoengineering (CNN).

Dr. Felix Schuermann

Felix Schürmann is the General Project Manager of the Blue Brain Project and a scientist at the Brain Mind Institute at the EPFL. He started his studies of physics at the University of Heidelberg, Germany supported by the German National Academic Foundation. He obtained his master's degree (M.S.) in physics from the State University of New York, Buffalo, USA, under the supervision of Richard Gonsalves. During this time he was a Fulbright Scholar. His master thesis dealt with the foundations of computing: the simulation of quantum computing. He received his Ph.D. in physics from the University of Heidelberg, Germany under the supervision of Karlheinz Meier in 2005. The focus of his work was on alternative approaches to computing: Using mixed-signal VLSI he co-designed an efficient implementation of a neural network in hardware and was the first to adopt "Liquid Computing" in hardware.

Dr. Johannes Schemmel

Johannes Schemmel received his diploma in physics and his Ph.D. degree in physics from the University of Heidelberg, Heidelberg, Germany, in 1997 and 1999, respectively. Since 1995 he works in the ASIC laboratory of the Kirchhoff Institute for physics which he is heading since 2008. His research interests include mixed-mode VLSI systems for image processing, image sensors, parallel analog computing, analog neural networks and hardware implementations of genetic algorithms. In recent years his research focus has concentrated in the area of biomorphic VLSI neural network models. His work in that area has contributed to the formation of the European research project "FACETS" where he is responsible for the development of a large distributed VLSI model of the vertebrate cortex that is based on wafer-scale integration.